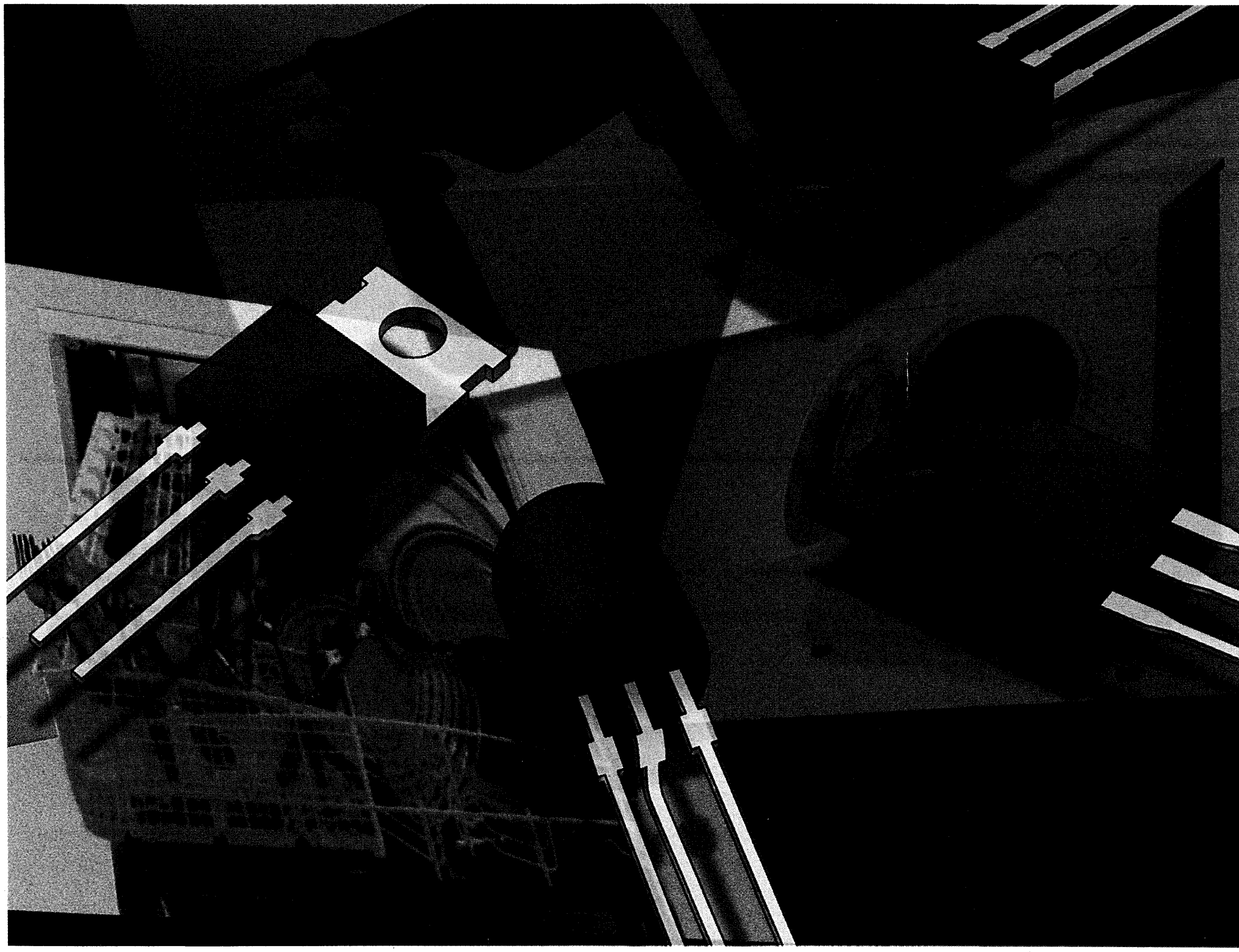
Thyristors and Triacs



1996

DATA HANDBOOK SC03

Philips
Semiconductors

PHILIPS

QUALITY ASSURED

Our quality system focuses on the continuing high quality of our components and the best possible service for our customers. We have a three-sided quality strategy: we apply a system of total quality control and assurance; we operate customer-oriented dynamic improvement programmes; and we promote a partnering relationship with our customers and suppliers.

PRODUCT SAFETY

In striving for state-of-the-art perfection, we continuously improve components and processes with respect to environmental demands. Our components offer no hazard to the environment in normal use when operated or stored within the limits specified in the data sheet.

Some components unavoidably contain substances that, if exposed by accident or misuse, are potentially hazardous to health. Users of these components are informed of the danger by warning notices in the data sheets supporting the components. Where necessary the warning notices also indicate safety precautions to be taken and disposal instructions to be followed. Obviously users of these components, in general the set-making industry, assume responsibility towards the consumer with respect to safety matters and environmental demands.

All used or obsolete components should be disposed of according to the regulations applying at the disposal location. Depending on the location, electronic components are considered to be 'chemical', 'special' or sometimes 'industrial' waste. Disposal as domestic waste is usually not permitted.

Thyristors and Triacs

CONTENTS

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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SELECTION GUIDE

SILICON BIDIRECTIONAL TRIGGER DEVICES

I_{FRM} (A)	$V_{(BO)}$ (V)	$I_{(BO)}$ (V)	TYPE NUMBER	ENVELOPE
2	28 - 36	50 µA	BR100/03	SOD27
2	28 - 36	50 µA	BR100/LLD	SOD80

STANDARD THYRISTORS

$I_{T(AV)}$ (A)	V_{DRM}, V_{RRM} (V)	I_{GT} MAX (mA)	TYPE NUMBER	ENVELOPE
5	500 600 800	15	BT300-500 BT300-600 BT300-800	TO220AB
5.7	500 650 800	15	BT151F-500 BT151F-650 BT151F-800	SOT186
5.7	500 650 800	15	BT151X-500 BT151X-650 BT151X-800	SOT186A
7.5	500 650 800	15	BT151-500R BT151-650R BT151-800R	TO220AB
13	400 600 800	32	BT152-400R BT152-600R BT152-800R	TO220AB
16	500 600 800	35	BT145-500R BT145-600R BT145-800R	TO220AB

SENSITIVE GATE THYRISTORS

$I_{T(AV)}$ (A)	V_{DRM}, V_{RRM} (V)	I_{GT} MAX (mA)	TYPE NUMBER	ENVELOPE
7.5	500 650 800	4	BTA151-500R BTA151-650R BTA151-800R	SOT82

LOGIC LEVEL THYRISTORS

$I_{T(AV)}$	V_{DRM}, V_{RRM}	I_{GT} MAX	TYPE NUMBER	ENVELOPE
(A)	(V)	(μA)		
0.5	200 400 600 800	200	BT149B BT149D BT149E BT149G	SOT54
0.5	200 400 600 800	20 - 200	BT168B BT168D BT168E BT168G	SOT54
0.5	200 400 600 800	200	BT169B BT169D BT169E BT169G	SOT54
0.5	200	200	2N5064	SOT54
0.6	200 400 600 800	20 - 200	BT168BW BT168DW BT168EW BT168GW	SOT223
0.6	400	200	BT169DW	SOT223
0.6	400 500 600	200	BT148W-400R BT148W-500R BT148W-600R	SOT223
2.5	400 500 600	200	BT148-400R BT148-500R BT148-600R	SOT82
2.5	500 600 800	200	BT150-500R BT150-600R BT150-800R	TO220AB
5	500 600 800	200	BT258-500R BT258-600R BT258-800R	TO220AB

STANDARD TRIACS

$I_{T(RMS)}$	V_{DRM}	I_{GT} MAX				TYPE NUMBER	ENVELOPE
(A)	(V)	(mA)					
		T2+ G+	T2+ G-	T2- G-	T2- G+		
1	500 600 800	35	35	35	70	BT134W-500 BT134W-600 BT134W-800	SOT223
4	500 600 800	35	35	35	70	BT134-500 BT134-600 BT134-800	SOT82
4	500 600 800	25	25	25	70	BT134-500F BT134-600F BT134-800F	SOT82
4	500 600 800	50	50	50	100	BT134-500G BT134-600G BT134-800G	SOT82
4	500 600 800	35	35	35	70	BT136-500 BT136-600 BT136-800	TO220AB
4	500 600 800	25	25	25	70	BT136-500F BT136-600F BT136-800F	TO220AB
4	500 600 800	50	50	50	100	BT136-500G BT136-600G BT136-800G	TO220AB
4	500 600 800	35	35	35	70	BT136F-500 BT136F-600 BT136F-800	SOT186
4	500 600 800	25	25	25	70	BT136F-500F BT136F-600F BT136F-800F	SOT186
4	500 600 800	50	50	50	100	BT136F-500G BT136F-600G BT136F-800G	SOT186
4	500 600 800	35	35	35	70	BT136X-500 BT136X-600 BT136X-800	SOT186A
4	500 600 800	25	25	25	70	BT136X-500F BT136X-600F BT136X-800F	SOT186A
4	500 600 800	50	50	50	100	BT136X-500G BT136X-600G BT136X-800G	SOT186A

STANDARD TRIACS (continued)

$I_{T(RMS)}$ (A)	V_{DRM} (V)	I_{GT} MAX (mA)				TYPE NUMBER	ENVELOPE
		T2+ G+	T2+ G-	T2- G-	T2- G+		
8	500 600 800	35	35	35	70	BT137-500 BT137-600 BT137-800	TO220AB
8	500 600 800	25	25	25	70	BT137-500F BT137-600F BT137-800F	TO220AB
8	500 600 800	50	50	50	100	BT137-500G BT137-600G BT137-800G	TO220AB
8	500 600 800	35	35	35	70	BT137F-500 BT137F-600 BT137F-800	SOT186
8	500 600 800	25	25	25	70	BT137F-500F BT137F-600F BT137F-800F	SOT186
8	500 600 800	50	50	50	100	BT137F-500G BT137F-600G BT137F-800G	SOT186
8	500 600 800	35	35	35	70	BT137X-500 BT137X-600 BT137X-800	SOT186A
8	500 600 800	25	25	25	70	BT137X-500F BT137X-600F BT137X-800F	SOT186A
8	500 600 800	50	50	50	100	BT137X-500G BT137X-600G BT137X-800G	SOT186A

STANDARD TRIACS (continued)

$I_{T(RMS)}$ (A)	V_{DRM} (V)	I_{GT} MAX (mA) T2+ G+	T2+ G-	T2- G-	T2- G+	TYPE NUMBER	ENVELOPE
12	500 600 800	35	35	35	70	BT138-500 BT138-600 BT138-800	TO220AB
12	500 600 800	25	25	25	70	BT138-500F BT138-600F BT138-800F	TO220AB
12	500 600 800	50	50	50	100	BT138-500G BT138-600G BT138-800G	TO220AB
12	500 600 800	35	35	35	70	BT138F-500 BT138F-600 BT138F-800	SOT186
12	500 600 800	25	25	25	70	BT138F-500F BT138F-600F BT138F-800F	SOT186
12	500 600 800	50	50	50	100	BT138F-500G BT138F-600G BT138F-800G	SOT186
12	500 600 800	35	35	35	70	BT138X-500 BT138X-600 BT138X-800	SOT186A
12	500 600 800	25	25	25	70	BT138X-500F BT138X-600F BT138X-800F	SOT186A
12	500 600 800	50	50	50	100	BT138X-500G BT138X-600G BT138X-800G	SOT186A

STANDARD TRIACS (continued)

$I_{T(RMS)}$ (A)	V_{DRM} (V)	I_{GT} MAX (mA) T2+ G+	T2+ G-	T2- G-	T2- G+	TYPE NUMBER	ENVELOPE
16	500 600 800	35	35	35	70	BT139-500 BT139-600 BT139-800	TO220AB
16	500 600 800	25	25	25	70	BT139-500F BT139-600F BT139-800F	TO220AB
16	500 600 800	50	50	50	100	BT139-500G BT139-600G BT139-800G	TO220AB
16	500 600 800	35	35	35	70	BT139F-500 BT139F-600 BT139F-800	SOT186
16	500 600 800	25	25	25	70	BT139F-500F BT139F-600F BT139F-800F	SOT186
16	500 600 800	50	50	50	100	BT139F-500G BT139F-600G BT139F-800G	SOT186
16	500 600 800	35	35	35	70	BT139X-500 BT139X-600 BT139X-800	SOT186A
16	500 600 800	25	25	25	70	BT139X-500F BT139X-600F BT139X-800F	SOT186A
16	500 600 800	50	50	50	100	BT139X-500G BT139X-600G BT139X-800G	SOT186A

STANDARD TRIACS (continued)

$I_{T(RMS)}$ (A)	V_{DRM} (V)	I_{GT} MAX (mA) T2+ G+	T2+ G-	T2- G-	T2- G+	TYPE NUMBER	ENVELOPE
25	500 600 800	35	35	35	70	BTA140-500 BTA140-600 BTA140-800	TO220AB

HIGH COMMUTATION TRIACS

$I_{T(RMS)}$ (A)	V_{DRM} (V)	I_{GT} MAX (mA) T2+ G+	T2+ G-	T2- G-	T2- G+	TYPE NUMBER	ENVELOPE
8	600 800	50	50	50	-	BTA208-600B BTA208-800B	TO220AB
8	600 800	50	50	50	-	BTA208X-600B BTA208X-800B	SOT186A
12	600 800	50	50	50	-	BTA212-600B BTA212-800B	TO220AB
12	600 800	50	50	50	-	BTA212X-600B BTA212X-800B	SOT186A
16	600 800	50	50	50	-	BTA216-600B BTA216-800B	TO220AB
16	600 800	50	50	50	-	BTA216X-600B BTA216X-800B	SOT186A
25	600 800	50	50	50	-	BTA225-600B BTA225-800B	TO220AB

HIGH NOISE IMMUNITY TRIACS

$I_{T(RMS)}$ (A)	V_{DRM} (V)	I_{GT} MIN-MAX (mA) T2+ G+	T2+ G-	T2- G-	T2- G+	TYPE NUMBER	ENVELOPE
16	500 600 800	10-50	10-50	10-50	10-100	BT139-500H BT139-600H BT139-800H	TO220AB
16	500 600 800	10-50	10-50	10-50	10-100	BT139F-500H BT139F-600H BT139F-800H	SOT186
16	500 600 800	10-50	10-50	10-50	10-100	BT139X-500H BT139X-600H BT139X-800H	SOT186A

SENSITIVE GATE TRIACS

$I_{T(RMS)}$ (A)	V_{DRM} (V)	I_{GT} MAX (mA)				TYPE NUMBER	ENVELOPE
		T2+ G+	T2+ G-	T2- G-	T2- G+		
1	500 600	10	10	10	25	BT134W-500E BT134W-600E	SOT223
4	500 600 800	10	10	10	25	BT134-500E BT134-600E BT134-800E	SOT82
4	500 600 800	10	10	10	25	BT136-500E BT136-600E BT136-800E	TO220AB
4	500 600 800	10	10	10	25	BT136F-500E BT136F-600E BT136F-800E	SOT186
4	500 600 800	10	10	10	25	BT136X-500E BT136X-600E BT136X-800E	SOT186A
8	500 600 800	10	10	10	25	BT137-500E BT137-600E BT137-800E	TO220AB
8	500 600 800	10	10	10	25	BT137F-500E BT137F-600E BT137F-800E	SOT186
8	500 600 800	10	10	10	25	BT137X-500E BT137X-600E BT137X-800E	SOT186A
12	500 600 800	10	10	10	25	BT138-500E BT138-600E BT138-800E	TO220AB
12	500 600 800	10	10	10	25	BT138F-500E BT138F-600E BT138F-800E	SOT186
12	500 600 800	10	10	10	25	BT138X-500E BT138X-600E BT138X-800E	SOT186A
16	500 600 800	10	10	10	25	BT139-500E BT139-600E BT139-800E	TO220AB
16	500 600 800	10	10	10	25	BT139F-500E BT139F-600E BT139F-800E	SOT186
16	500 600 800	10	10	10	25	BT139X-500E BT139X-600E BT139X-800E	SOT186A

LOGIC LEVEL TRIACS

$I_{T(RMS)}$	V_{DRM}	I_{GT} MAX				TYPE NUMBER	ENVELOPE
(A)	(V)	(mA)					
		T2+ G+	T2+ G-	T2- G-	T2- G+		
1	500 600	5	5	5	10	BT134W-500D BT134W-600D	SOT223
1	500 600	5	5	5	10	BT134-500D BT134-600D	SOT82
4	500 600	5	5	5	10	BT136-500D BT136-600D	TO220AB
4	500 600	5	5	5	10	BT136F-500D BT136F-600D	SOT186
4	500 600	5	5	5	10	BT136X-500D BT136X-600D	SOT186A
8	500 600	5	5	5	10	BT137-500D BT137-600D	TO220AB
8	500 600	5	5	5	10	BT137F-500D BT137F-600D	SOT186
8	500 600	5	5	5	10	BT137X-500D BT137X-600D	SOT186A

INTRODUCTION

NEW PRODUCTS

Philips Semiconductors are working intensively on bringing new products to the market to meet the requirements of existing and new developing applications areas. These are the new products and technologies that appear for the first time in this data handbook.

HIGH COMMUTATION TRIACS

Philips range of high commutation triacs now include two new devices rated at 8 A and 25 A. These devices have high off-state dV/dt and commutation capability, and are ideal for use in motor control circuits and other inductive switching applications. (Types: BTA208, BTA225).

ISOLATED THYRISTORS AND TRIACS

The Industry Standard - BT151 thyristor plus a wide range of standard and high-commutation triacs are now available in the SOT186A isolated package, featuring isolation voltage up to 2500 Vrms. The SOT186A package allows two or more power devices to share a common heatsink, without the need for insulating bushes and spacers, or alternatively allows the heatsink to be grounded. (Types: BT151X, BT136X, BT137X, BT138X, BT139X, BTA208X, BTA212X, BTA216X).

SURFACE MOUNTING BT169

The popular BT169D, sensitive gate thyristor, used in a wide variety of consumer applications is now available in a SOT223 envelope, suitable for surface mounting (Type: BT169DW).

NEW 5 A RATED THYRISTOR

The BT300 series is a range of 5 A rated thyristors with similar characteristics to the BT151, available in 500 V, 600 V and 800 V grades. It is intended for lower power applications where the 7.5 A rating of the BT151 is not required (Types: BT300-500R, BT300-600R, BT300-800R).

NEW 5 A RATED, LOGIC LEVEL THYRISTOR

The BT258 series is a range of 5 A rated, sensitive gate thyristors available in 500 V, 600 V and 800 V grades. The BT258 may be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits. This device is particularly suitable for microprocessor controlled domestic appliances and low power consumer products. (Types: BT258-500R, BT258-600R, BT258-800R)

ADDITIONAL VOLTAGE GRADES FOR BT150

Up to now, the BT150 has only been available in the 500 V grade. Additional voltage grades of 600 V and 800 V are now available. (Types: BT150-600R, BT150-800R)

UNENCAPSULATED, PASSIVATED, SILICON POWER CHIPS

All the devices in this data handbook are available as unencapsulated dice complete with passivation and metallised contact pads, but without bond wires or any other connections or encapsulation. Contact your Regional or National Sales Office for details.

APPLICATIONS

For further information on applications which use thyristors and triacs, refer to the new handbook "Triacs and thyristors - an application guide" (Order code: 9397-750-00372).

For further information on other power semiconductor applications, refer to the "Power Semiconductor Applications Handbook" (Order code:9398-652-85011).

PHILIPS THYRISTORS AND TRIACS

The Phase 2 Process

The basic principle of using a PNPN structure to produce a thyristor, and a NPNPN structure (with two PNPN's in antiparallel) to produce a triac has been known for decades. The factors controlling various important parameters, such as blocking voltages, on-state voltage drop, trigger current, latching and holding current, off-state dV/dt, triac commutation and surge capability are also well known.

The modern challenge of making good thyristors and triacs lies not so much in innovative design concepts as in perfection of manufacturing technology.

Philips products are characterised by the use of well established, stable processes in both diffusion and assembly, giving devices of high quality and reliability. The strengths and special features of these products are outlined below.

Except for those designed for specialist applications such as GTO's and ASCR's, most common thyristors and triacs are specified to have voltage blocking capability in both directions. This means that in the PNPN or NPNPN structures, two opposing PN junctions need to be designed to withstand the rated voltage.

This is normally achieved by starting with a suitably low doped N type silicon wafer into which two P regions are diffused simultaneously from opposite sides, resulting in a symmetric PNP structure where both PN junctions have high voltage blocking capability. Further N-type diffusions are then put into both sides of the structure, (for a triac). The result is a NPNPN structure with a symmetrical blocking voltage. Both of these blocking PN junctions now need to be passivated at the point where they intersect the silicon surface, and there are two common methods for doing this, shown in the diagrams below.

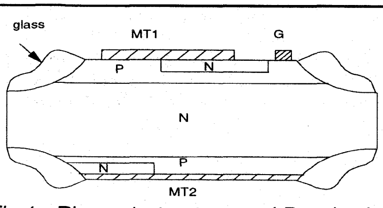


Fig.1. Phase 1 structure and Passivation.

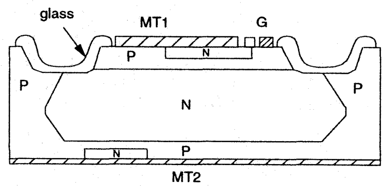


Fig.2. Phase 2 structure and Passivation.

In Philips terminology we call these "Phase 1" and "Phase 2" technologies respectively.

As can be seen, Phase 1 passivation requires a simultaneous etching of mesa troughs from both sides followed by the deposition of passivants such as negatively charged glass. The advantages of this technique are small chip size and fewer processing stages. No aluminium isolation diffusion or photolith are required, hence the overall chip cost is lower.

By contrast, the Phase 2 technology requires an aluminium isolation diffusion prior to the fabrication of the PNPN or NPNPN structure, which has the effect of bringing both blocking PN junctions to the top surface. These can then be passivated with trough etching and glass deposition on the top side only.

The main advantage of the Phase 2 technology is a much more mechanically robust structure, due to the fact that the edge of the chip is not reduced in thickness. Minor damage to the edges does not intrude into the active region. A further advantage is that the flat bottom surface is compatible with automatic die bonding in assembly.

The main disadvantage is increased cost in comparison with the Phase 1 process.

Philips has progressed from Phase 1 to Phase 2 passivation technology, despite its higher cost, because of the advantages of mechanical ruggedness and lower vulnerability to handling damage.

It is our belief that Philips thyristors and triacs produced using Phase 2 technology have fewer manufacturing defects, and are more reliable than devices produced by competitors who are still using the Phase 1 structure.

Passivation

The use of the Phase 2 passivation structure coupled with the well developed glass mesa passivation technology at Philips results in devices with high voltage blocking capability and extremely stable characteristics. The structure is also less vulnerable to edge damage compared to the alternative Phase 1 passivation.

The typical off-state breakdown voltage of our thyristors and triacs is in excess of 1000V, with a very tight distribution, so much so that we normally consider any devices with blocking voltages less than 500V to be defective. For example, our 200V and 400V grade devices are tested to withstand 500V.

In contrast, competitors using Phase 1 passivation who deliver true 200V and 400V devices, i.e. devices whose breakdown voltages are just above 200V or 400V, are likely to suffer from glass cracks or chipped corners which can progress to the extent that they cause quality and reliability problems.

Assembly

The absence of troughs and glass on the bottom surface of our chips allows us to use automated assembly. We use die bonding technology which involves scrubbing the chips onto heated leadframes that are precoated with solder. This technique gives an excellent, void free contact with low thermal resistance and avoids having to subject the chips to long duration, high temperature furnacing. Compared to our main competitors, our devices have superior die bonds and lower thermal resistance, which means that they operate at a lower junction temperature for the same dissipation, and thus have higher reliability.

Another feature of this assembly method is that, along with the ultrasonic wire bonding used to connect to the top of the chip, it gives our devices a high thermal fatigue capability. Thus they have excellent on-state reliability as well as extremely stable off-state characteristics.

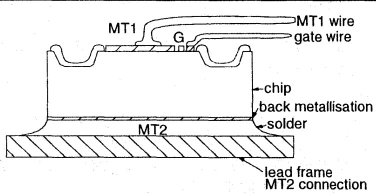


Fig.3. Die bonding onto leadframes, wire bonding.

Unencapsulated Dice

Because of the advantages of the Philips process and assembly techniques outlined above, our family of triacs and thyristors are ideal for use in unencapsulated form, in applications where space and height are at a premium. The glass passivation protects the, otherwise exposed surface regions giving highly stable device characteristics. The silicon wafers are 100% electrically tested and are normally supplied sawn, on blue film frame carriers. Unsawn wafers can be supplied where necessary.

Philips Semiconductors have a wealth of experience of supplying devices in this form and are able to provide expert advice on the subject of mounting, soldering and attaching bond wires to unpackaged dice.

Thyristor and Triac Ratings

A rating is a value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

All limiting values quoted in this data handbook are Absolute Maximum Ratings - limiting values of operating and environmental conditions applicable to any device of a specified type, as defined by its published data.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value is exceeded with any device, under the worst probable operating conditions.

VOLTAGE RATINGS

V_{DRM}, V_{RRM} — Repetitive peak off-state voltage. The maximum allowable instantaneous forward or reverse voltage including transients. The rated values of $V_{DRM(max)}$ and $V_{RRM(max)}$ may be applied continuously over the entire operating junction temperature range, provided that the thermal resistance between junction and ambient is kept low enough to avoid the possibility of thermal runaway.

CURRENT RATINGS

$I_{T(AV)}$ — Average on-state current. The average rated current is that value which under steady state conditions will result in the rated temperature T_{jmax} being reached when the mounting base or heatsink is at a given temperature. Graphs of on-state dissipation versus $I_{T(AV)}$ or $I_{T(RMS)}$ are provided in the data sheets. The right hand scale of each graph shows the maximum allowable mounting base or heatsink temperature for a given dissipation.

$I_{T(RMS)}$ — RMS on-state current. For a given average current, the power dissipated at small conduction angles is much higher than at large conduction angles. This is a result of the higher rms currents at small conduction angles. Operating the device at rms currents above the rated value is likely to result in rapid thermal cycling of the chip and the bond wires which can lead to reliability problems.

I_{TSM} — Non-repetitive peak on-state current. The maximum allowable peak, on-state surge current which may be applied no more than 100 times in the life of the device. The data sheet condition assumes a starting junction temperature equal to T_{jmax}, and a sinusoidal surge current at a mains frequency of 50/ 60 Hz. For a triac, a full sine wave of current is applied.

Immediately after the surge, the mains voltage is reapplied with a peak value equal to the full rated off-state voltage, V_{DRM}. Graphs in the data sheet show the variation of I_{TSM} with surge duration.

I^2t — Device fuse rating. For correct circuit protection, the I^2t of a protective fuse must be less than the I^2t of the device. In the data sheets, the device rating is numerically equal to $I_{TSM}{}^2/200$ and assumes a 10ms fusing time.

dI_T/dt — The maximum allowable rate of rise of on-state current after gate triggering. The theory underlying this rating is that, where the rate of rise of main current is very rapid immediately after triggering, local 'hot spot' heating will occur in a small part of the device active area close to the gate, leading to device degradation or complete failure. In practise, true dI_T/dt failures of this kind are very rare. The only conditions where dI_T/dt has been observed to cause failures is in triacs operated in the T2-, G+ quadrant where a combination of high dI_T/dt and high peak current (in excess of the data sheet ratings), can cause damage to the gate structure. For this reason, operation of our triacs in the T2-, G+ quadrant should be avoided wherever possible.

dI_T/dt — V_{BO} or dV_D/dt triggered. Where a device is triggered by exceeding the breakdown voltage, or by a high rate of rise of off-state voltage, as opposed to injecting current into the gate, it is necessary to limit the dI_T/dt. A note in the data sheet specifies the maximum allowable dI_T/dt for this mode of triggering.

THERMAL RATINGS

$R_{th\ j\text{-}mb}$, $R_{th\ j\text{-}hs}$, $R_{th\ j\text{-}sp}$, $R_{th\ j\text{-}lead}$ — Steady state thermal resistances. Junction to mounting base is used for TO220AB envelope. Junction to heatsink for devices in full pack, isolated envelopes, SOT186 and SOT186A. Junction to solder point is used for devices in SOT223 surface mounting envelope. Junction to lead is used for devices in SOT54 (TO92) small signal outline. The maximum value of the thermal resistance is given in the data sheet, and is used to specify the device rating. The average junction temperature rise for a given dissipation is given by multiplying the average dissipation by the thermal resistance.

Note that for triacs, two values of thermal resistance are quoted; one for half cycle operation and one for full cycle operation. This is because only half of the chip carries current in each half cycle allowing the non-conducting half to cool down between conduction periods. The net effect is to reduce the average thermal resistance for full cycle conduction.

$R_{th\ j\text{-}a}$ — Typical values of junction to ambient thermal resistance are given in the data sheet assuming that the device is mounted vertically on a printed circuit board, in free air.

$Z_{th\ j\text{-}mb}$, $Z_{th\ j\text{-}hs}$ — Whilst the average junction temperature rise may be found from the thermal resistance figure, the peak junction temperature requires knowledge of the current waveform and the transient thermal impedance. The thermal impedance curves in the data sheets are based on rectangular power pulses. The junction temperature rise due to a rectangular power pulse, is given by multiplying the peak dissipation during the pulse by the thermal impedance $Z_{th\ j\text{-}mb}$ for the given pulse width. Analysis methods for non-rectangular pulses are covered in the Power Semiconductor Applications handbook.

T_{jmax} — The maximum operating junction temperature range for all our thyristors and triacs is 125˚C. This applies in either the on-state or off-state, and for either half cycle or full cycle conduction. It is permissible for the junction temperature to exceed $T_{j\ max}$ for short periods during non-repetitive surges, but for repetitive operation the peak junction temperature must remain below $T_{j\ max}$.

T_{stg} — The limiting storage temperature range for all our thyristors and triacs is -40˚C to 150˚C.

$P_{G(AV)}$, P_{GM}, I_{GM}, V_{GM} — The average and peak gate power dissipation, and the maximum gate voltage and gate current. Exceeding the gate ratings can cause the device to degrade gradually, or fail completely.

Thyristor and Triac Characteristics

A characteristic is an inherent and measurable property of a device. Such a property may be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

STATIC CHARACTERISTICS

V_T — On-state voltage. The tabulated value in the data sheet is the maximum, instantaneous on-state voltage measured under pulse conditions to avoid excessive dissipation, at a junction temperature of 25˚C. The data sheet also contains a graph showing the maximum and typical characteristics at 125˚C and the maximum characteristic at 25˚C. The maximum characteristic at 125˚C is used to calculate the dissipation for a given average or rms current, and hence the graph of on-state dissipation versus average or rms current in the data sheet.

The on-state voltage/ current characteristic of a diode, thyristor or triac may be approximated by a piecewise linear model as shown in the figure below; where R_S is the slope of the tangent to the curve at the rated current, and V_O is the voltage axis intercept. The on-state voltage is then $V_T = V_O + I_T.R_S$, and the instantaneous dissipation is $P_T = V_O.I_T + I_T^2.R_S$. where I_T is the instantaneous on-state current.

It can be shown that the average on-state dissipation for any current waveform is: $P_{T(AV)} = V_O.I_{T(AV)} + I_{T(RMS)}^2.R_S$, where $I_{T(AV)}$ is the average on-state current and $I_{T(RMS)}$ is the rms value of the on-state current. Graphs in the published data show on-state dissipation as a function of average current for thyristors and versus rms current for triacs. Sinusoidal current waveforms are assumed and the graphs show dissipation over a range of conduction angles

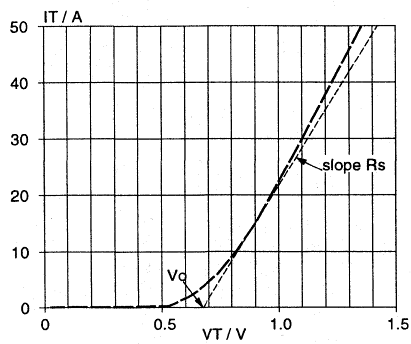


Fig.4. Piecewise linear approximation to thyristor and triac on-state characteristic.

I_{GT} Gate trigger current. The data sheet shows the typical and maximum gate trigger current at a junction temperature of 25˚C. A graph in the data sheet shows the variation of normalised I_{GT} with temperature.

When designing a triac gate trigger circuit, triggering in the T2-, G+ quadrant should be avoided if possible. The gate trigger current in this quadrant is much higher than in the other three quadrants and the device is more susceptible to turn-on dI_T/dt failure.

V_{GT} Gate trigger voltage. The data sheet shows the typical and maximum gate trigger voltage at a gate current equal to I_{GT}, at a junction temperature of 25˚C. A graph in the data sheet shows the variation of normalised V_{GT} with temperature.

To ensure that a device will not trigger, the gate voltage must be held below the minimum gate trigger voltage. The data sheet quotes $V_{GT(min)}$ at the maximum junction temperature (125˚C), and the maximum off-state voltage ($V_{DRM(max)}$).

I_L Latching current. The latching current is the value of on-state current required to maintain conduction at the instant when the gate current is removed. A graph in the data sheets shows the variation of normalised I_L with temperature.

To trigger a thyristor or triac, a gate current greater than the maximum device gate trigger current I_{GT} must be applied until the on-state current I_T rises above the maximum latching current I_L. This condition must be met at the lowest junction temperature.

I_H Holding current. The holding current is the value of on-state current required to maintain conduction once the device has fully turned on and the gate current has been removed. The on-state current must have previously exceeded the latching current I_L. A graph in the data sheet shows the variation of normalised I_H with temperature.

To turn off (commutate) a thyristor or triac, the load current must remain below I_H for sufficient time to allow a return to the off-state. This condition must be met at the highest operating junction temperature (125˚C).

I_D, I_R The maximum off-state leakage current, specified at rated $V_{DRM(max)}$, $V_{RRM(max)}$ at 125˚C.

DYNAMIC CHARACTERISTICS

dV_D/dt Critical rate of rise of off-state voltage. Displacement current caused by a high rate of rise of off-state voltage can induce a gate current sufficient to trigger the device. Devices with sensitive gates are particularly susceptible to dV_D/dt triggering, and since gate trigger current decreases as junction temperature increases, the condition is worse when the device is hot. The data sheet figure is specified at 125˚C using an exponential waveform and a maximum applied voltage of 67% $V_{DRM(max)}$. The dV_D/dt is measured to 63% of the maximum voltage.

To prevent sensitive gate devices from false triggering due to high rates of rise of off state voltage, 1 kΩ resistor in parallel with a 10nF capacitor may be fitted between gate and cathode (gate and terminal 1 for a triac). This approach is less effective for standard gate devices. In this case, the preferred option is to fit an RC snubber between anode and cathode (T2 and T1 for a triac) to reduce the dV_D/dt below the critical value.

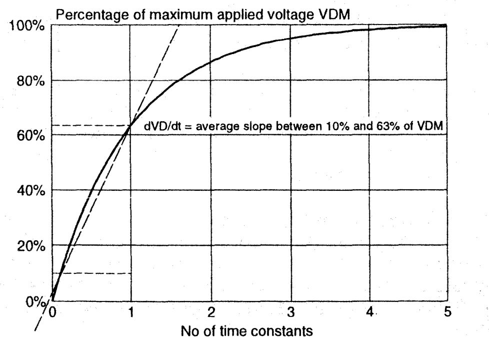


Fig.5. Exponential waveform used for measurement of critical off-state dV_D/dt. The dV_D/dt is the average slope between 10% and 63% of the maximum applied voltage V_{DM}.

t_{gt} Gate controlled turn-on time. A typical turn on time of 2 μs is specified for all our thyristors and triacs.

t_q Circuit commutated turn-off time. A typical turn off time of 70 μs is specified for standard gate thyristors and 100μs for sensitive gate thyristors.

TRIAC COMMUTATION

A triac is an AC conduction device and may be thought of as two thyristors in antiparallel, monolithically integrated onto the same silicon chip. In phase control circuits, the triac often has to be triggered into conduction part way into each half cycle. This means that at the end of each half cycle the on-state current in one direction must drop to zero and not resume in the other direction until the device is triggered again. This commutation turn-off capability is at the heart of triac power control applications. If the triac were truly two separate thyristors in antiparallel, this requirement would not present any problems. However, as the two are on the same piece of silicon there is the possibility that the unrecombined charge of one thyristor as it turns off may act as gate current to trigger the other thyristor as the voltage rises in the opposite direction. This phenomenon is called commutation failure.

There are two components of current which can act as gate current to cause commutation failure. One of these is the displacement current generated by the reapplied dV_{com}/dt. The other is the recombination current, which is mainly determined by the rate of fall of commutating current, dI_{com}/dt. Both tend to create a lateral volt drop in the emitter of the opposing thyristor which triggers the device in the opposite direction to the original current flow.

At low rates of fall of current, dI_{com}/dt, the ammount of unrecombined charge is small and commutation failure occurs mainly because of the rate of rise of off-state voltage, dV_{com}/dt. This situation is worst for inductive loads where the rate of rise of voltage can be very high when commutation occurs. The conventional remedy for this type of commutation failure is to fit a snubber across the device to limit the rate of rise of off-state voltage dV_{com}/dt.

At high values of dI_{com}/dt, the recombination current dominates and, above a critical value of dI_{com}/dt, the device will not commutate even at fairly low values of dV_{com}/dt. Under these conditions, a snubber will not prevent commutation failure, and the best option is to use a High Commutation Triac.

HIGH COMMUTATION TRIACS

Philips High Commutation Triacs attempt to separate the two antiparallel thyristor structures to prevent the unrecombined charge from the conducting half becoming gate current in the other half. This is accomplished by lateral separation of the top and bottom emitters, more extensive emitter and peripheral shorting, and by a modified gate design which prevents triggering in the T2-, G+ quadrant.

The device design, in addition to giving high immunity to commutation failure, also improves the off-state dV_D/dt capability. They will commutate the full rated current up to 125˚C without the aid of a snubber and will also withstand extremely high rates of rise of off-state voltage, in excess of 1000 V/μs. High commutation triacs can simplify circuit design by eliminating the need for RC snubbers. Typical applications include; motor starting, where the triac may be required to commutate the starting current; the switching of d.c. operated relay coils where the time constant of the coil is much greater than the mains period and static switching where it is required to turn the triac off whilst it is carrying an overload current.

dV_{com}/dt Critical rate of rise of commutating voltage. For conventional, as opposed to high commutation triacs, the data sheet conditions specify a junction temperature of 95˚C and a dI_{com}/dt given by $2.\sqrt{2}.\pi.f.I_{T(RMS)}$, where f is the mains frequency (assumed to be 50Hz). This value is the maximum rate of change of current which occurs at the zero crossing for a sine wave current equal to the rated rms value, $I_{T(RMS)}$. Graphs in the data sheet show the variation of dV_{com}/dt and with junction temperature with dI_{com}/dt as a parameter.

dI_{com}/dt Critical rate of change of commutating current. High Commutation Triacs are intended for use in circuits where high values of both dI_{com}/dt and dV_{com}/dt can occur. Commutation capability is specified in terms of dI_{com}/dt, without a snubber and at the highest junction temperature, T_{jmax} = 125˚C. A graph in the data sheet shows the variation of dI_{com}/dt with junction temperature.

Operation up to 150˚C

The maximum operating junction temperature, T_{jmax} of Philips thyristors and triacs is 125˚C. Operation above T_{jmax} for long periods, particularly in the off-state, can give rise to reliability problems due to changes in characteristics which occur as a result of mobile charge in the glass passivation.

Furthermore, as a thyristor or triac gets hot, it becomes more susceptible to false gate triggering, off-state dV_D/dt triggering, thermal runaway and commutation failure.

However, it has become apparent that some customers have applications which require operation of thyristors and triacs at higher junction temperatures.

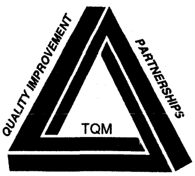
Recent improvements in Philips glass mesa technology backed up by extensive reliability testing has shown that, for certain applications, our thyristors and triacs can be operated reliably at junction temperatures up to 150˚C.

Typical applications where 150˚C operation may be allowed include:- static switching of resistive loads, power switches for domestic appliances and electric heating applications where the device is mounted on a high temperature substrate.

Extending the upper operating junction temperature to 150˚C depends very much on the application. For this reason we recommend that customers wishing to use our thyristors and triacs at 150˚C contact the Field Applications Engineer at their Regional or National sales office.

QUALITY

Total Quality Management



QUALITY ASSURANCE SYSTEM

Philips Semiconductors is committed to be a world class, customer driven, volume supplier of semiconductors.

To achieve this, we operate a Total Quality Management (TQM) system, based on Continuous Improvement and Quality Assurance in all our business activities, and Partnerships with our customers and suppliers.

The top priority throughout the company is Continuous Improvement.

To focus on this we will:

- Work closely with key customers, as our partners.
- Monitor progress, using customer-driven data, of our product and services.
- Benchmark against the best.

Furthermore, all parts of the organisation must always demonstrate:

- The presence of a strong, management-led improvement structure.
- Commitment and participation in all areas.
- Measurable progress towards our Quality Improvement goals.

Organisation

An organisation is in place which ensures that personnel with the necessary organisational freedom and authority can identify and solve quality problems, prevent occurrence of product non-conformity and protect the customer from non-conforming product.

Design control

A comprehensive design and development procedure is in place which ensures that the requirements of good design practice are met.

Particular emphasis is placed on ensuring that the initial specification is agreed by the Customer and the Marketing and Development functions.

There are regular formal reviews of design progress to ensure that the initial specification will be met by the design.

Detailed measurements are made on initial samples to ensure that the initial specification has been met.

Process control

All processes which directly affect quality are carried out under controlled conditions. Documented work instructions are available for all production processes and the appropriate environmental controls are in place to ensure consistent processing. Monitoring of the product, processes and the environment takes place during production.

Approval exercises are run to ensure that new processes and new equipment perform at an acceptable level.

Written, photographic or visual standards are available at the appropriate points in the production processes.

Corrective action

Non-conforming product found in process is investigated and the root causes identified. Changes to product or process are then introduced to prevent recurrence of the problem.

Quality assurance

Based on ISO 9000 standards, customer standards such as Ford TQE. Our factories are certified to ISO 9000.

Partnerships with customers

These include: PPM co-operations, design-in agreements, ship-to-stock, just-in-time, self-qualification programmes and application support.

Partnerships with suppliers

In addition to ISO9000 audits and close monitoring of supplier delivery performance, we operate a Supplier Excellence Award scheme which requires suppliers and their sub-suppliers to use statistical process control, perform gauge studies and use failure mode and effect analysis (FMEA) techniques to identify and correct the root causes of quality and delivery problems.

Product reliability

With the increasing complexity of Original Equipment Manufacturer (OEM) equipment, component reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies result in design rules and process optimizations for the highest built-in product reliability. Highly accelerated tests are applied in order to evaluate the product reliability. Rejects from reliability tests and from customer complaints are submitted to failure analysis and the results applied to improve the product or process.

Customer responses

Our quality improvement depends on joint action with our customer. We need our customers inputs and we invite constructive comment on all aspects of our performance. Please contact your local sales representative.

Recognition

The high quality of our products and services is demonstrated by many Quality Awards granted by major customers and international organisations.

DEVICE DATA

in alphanumeric sequence

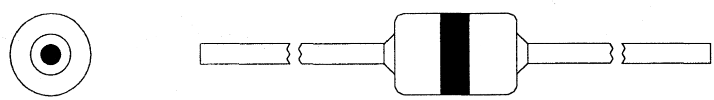
GENERAL DESCRIPTION

Silicon bidirectional trigger device in a glass envelope intended for use in triac and thyristor trigger circuits.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_{(BO)}$	Breakover voltage	28	36	V
V_O	Output voltage	7	-	V
I_{FRM}	Repetitive peak forward current	-	2	A

OUTLINE - SOD27



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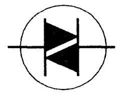


LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{FRM}	Repetitive peak forward current	$t \leq 10$ µs, $T_a \leq 50$˚C; f = 60 Hz	-	2	A
P_{tot}	Total power dissipation	$T_a = 50$˚C	-	150	mW
T_{stg}	Storage temperature		-55	125	˚C
T_j	Operating junction temperature		-	100	˚C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	330	-	K/W
$R_{th\ j\text{-}lead}$	Thermal resistance junction to leads		-	150	-	K/W

CHARACTERISTICS

$T_a = 25$ ˚C unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BO)}$	Breakover voltage	$I = I_{(BO)}$	28	32	36	V
$\lvert V_{(BO)+}\rvert - \lvert V_{(BO)-}\rvert$	Breakover voltage symmetry	$I = I_{(BO)}$, see fig: 1	-	-	3.5	V
V_O	Output voltage	$R_L = 20\ \Omega$; Circuit of fig: 2	7	-	-	V
$I_{(BO)}$	Breakover current	$V = V_{(BO)}$	-	-	50	µA
$dV_{(BO)}/dT$	Temperature coefficient of $V_{(BO)}$		-	0.1	-	%/K
t_r	Risetime	$I_p = 0.5$ A; Circuit of fig: 2	-	1.5		µs

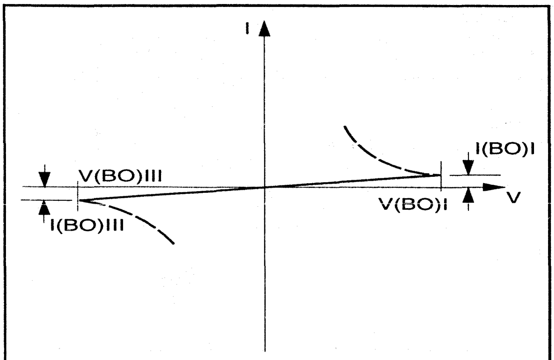


Fig.1. Current-voltage characteristics

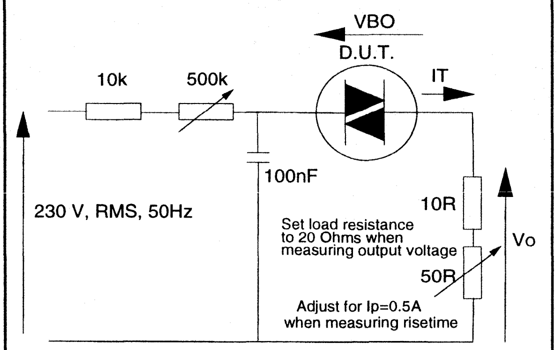


Fig.2. Test circuit for output voltage and risetime.

MECHANICAL DATA

Dimensions in mm

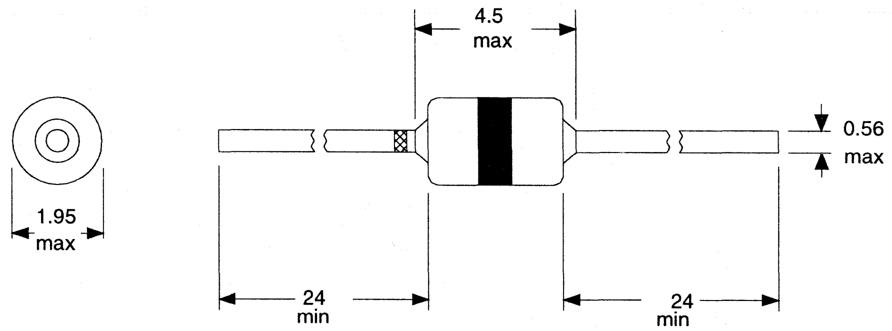


Fig.3. SOD27.

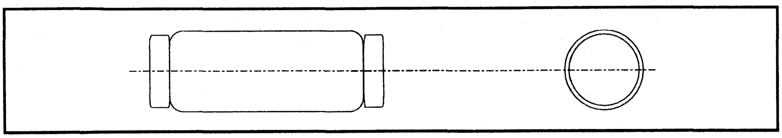
GENERAL DESCRIPTION

Silicon bidirectional trigger device in a glass envelope suitable for surface mounting. The device is intended for use in triac and thyristor trigger circuits.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_{(BO)}$	Breakover voltage	28	36	V
V_O	Output voltage	7	-	V
I_{FRM}	Repetitive peak forward current	-	2	A

OUTLINE - SOD80



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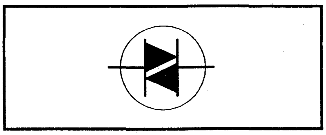


LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{FRM}	Repetitive peak forward current	$t \leq 10$ µs, $T_{tp} \leq 50$˚C; f = 60 Hz	-	2	A
P_{tot}	Total power dissipation	$T_{tp} = 50$˚C	-	150	mW
T_{stg}	Storage temperature		-55	125	˚C
T_j	Operating junction temperature		-	100	˚C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}tp}$	Thermal resistance junction to tie point	PCB mounted	-	330	-	K/W

CHARACTERISTICS

$T_a = 25$ ˚C unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BO)}$	Breakover voltage	$I = I_{(BO)}$	28	32	36	V
$\lvert V_{(BO)+}\rvert - \lvert V_{(BO)-}\rvert$	Breakover voltage symmetry	$I = I_{(BO)}$, see fig: 1	-	-	3.5	V
V_O	Output voltage	$R_L = 20\ \Omega$; Circuit of fig: 2	7	-	-	V
$I_{(BO)}$	Breakover current	$V = V_{(BO)}$	-	-	50	µA
$dV_{(BO)}/dT$	Temperature coefficient of $V_{(BO)}$		-	0.1	-	%/K
t_r	Risetime	$I_p = 0.5$ A; Circuit of fig: 2	-	1.5		µs

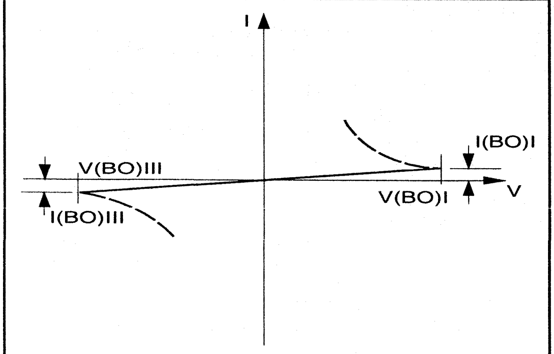


Fig.1. Current-voltage characteristics

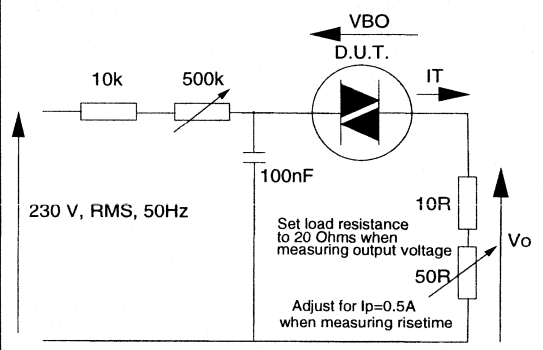


Fig.2. Test circuit for output voltage and risetime.

MECHANICAL DATA

Dimensions in mm

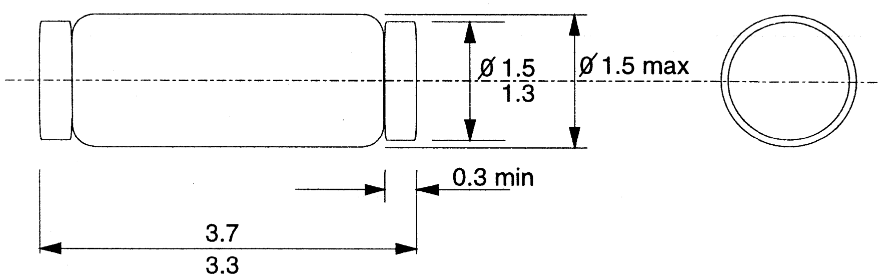


Fig.3. SOD80

GENERAL DESCRIPTION

Glass passivated triacs in a plastic envelope, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

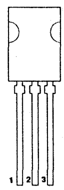
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT134-	500	600	800	
	BT134-	500F	600F	800F	
	BT134-	500G	600G	800G	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	4	4	4	A
I_{TSM}	Non-repetitive peak on-state current	25	25	25	A

PINNING - SOT82

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
tab	main terminal 2

PIN CONFIGURATION



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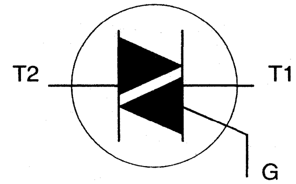


LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	-600	-800	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 107$ ˚C	-	4			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 20 ms	-	25			A
		t = 16.7 ms	-	27			A
I^2t	I^2t for fusing	t = 10 ms	-	3.1			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 6$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs					
		T2+ G+	-	50			A/µs
		T2+ G-	-	50			A/µs
		T2- G-	-	50			A/µs
		T2- G+	-	10			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	full cycle	-	-	3.0	K/W
		half cycle	-	-	3.7	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	100	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.			UNIT
		BT134-			...	...F	...G	
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A						
		T2+ G+	-	5	35	25	50	mA
		T2+ G-	-	8	35	25	50	mA
		T2- G-	-	11	35	25	50	mA
		T2- G+	-	30	70	70	100	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A						
		T2+ G+	-	7	20	20	30	mA
		T2+ G-	-	16	30	30	45	mA
		T2- G-	-	5	20	20	30	mA
		T2- G+	-	7	30	30	45	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	5	15	15	30	mA
V_T	On-state voltage	I_T = 5 A	-	1.4	1.70			V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5			V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-			V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5			mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.			TYP.	MAX.	UNIT
		BT134-	...	...F	...G			
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} =67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	100	50	200	250	-	V/µs
dV_{com}/dt	Critical rate of change of commutating voltage	V_{DM} = 400 V; T_j = 95 ˚C; $I_{T(RMS)}$ = 4 A; dI_{com}/dt = 1.8 A/ms; gate open circuit	-	-	10	50	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 6 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs;	-	-	-	2	-	µs

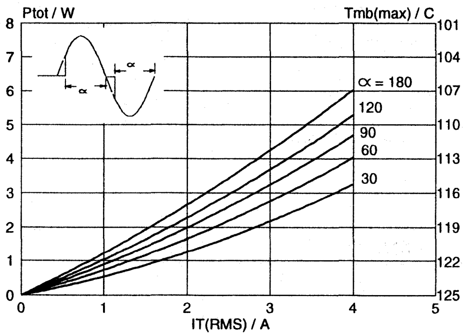


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

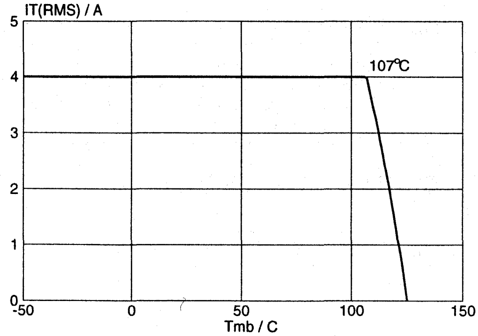


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

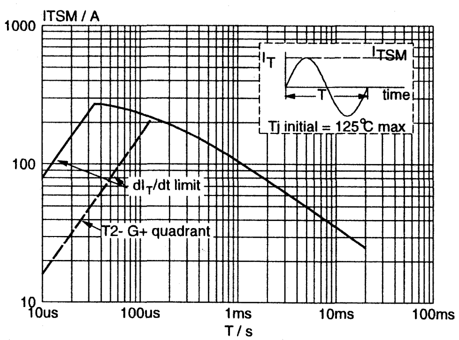


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

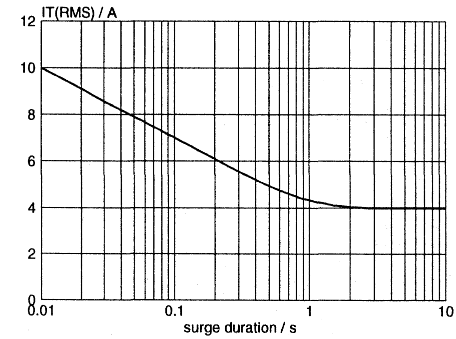


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 107$˚C.

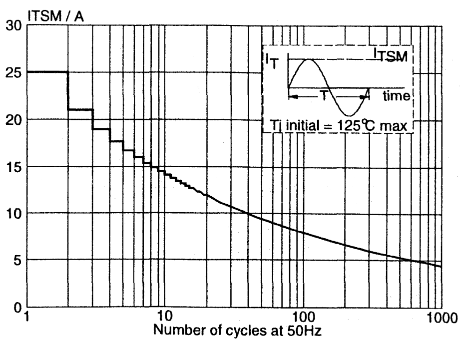


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

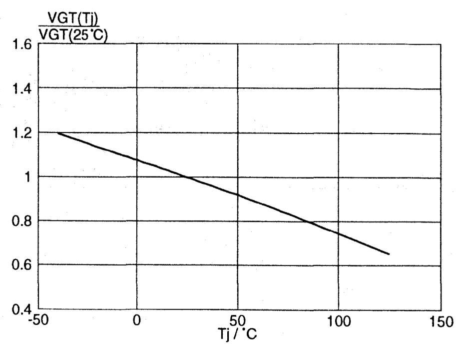


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25˚C)$, versus junction temperature T_j.

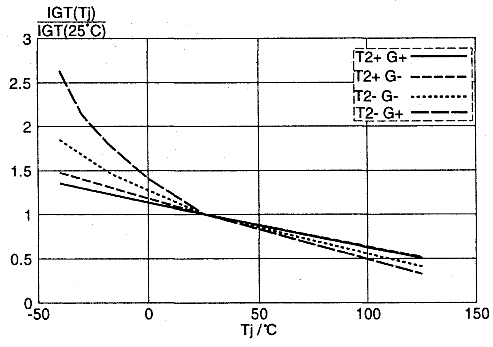


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

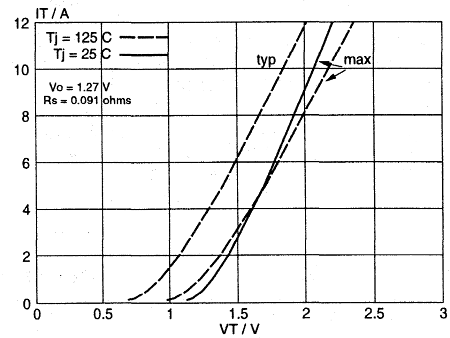


Fig.10. Typical and maximum on-state characteristic.

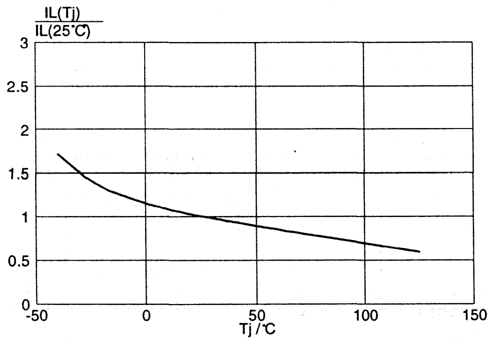


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.

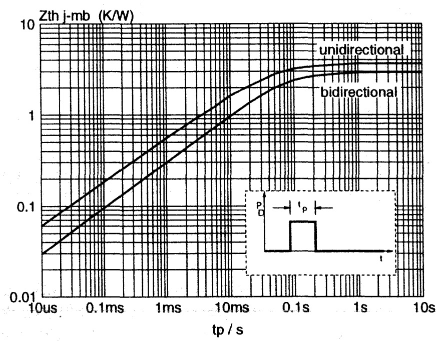


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width t_p.

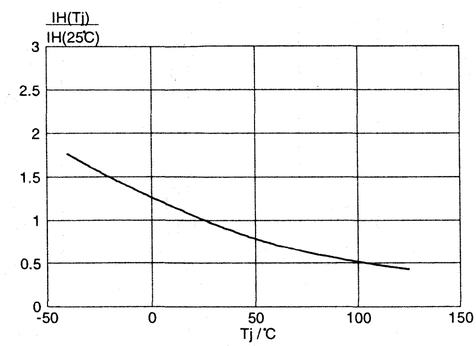


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j.

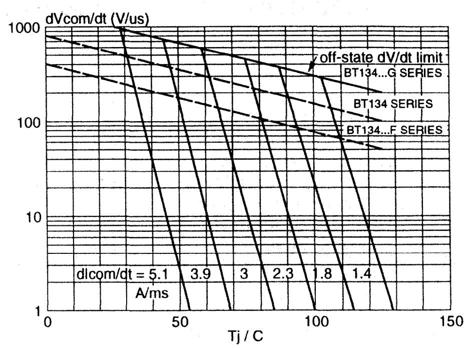


Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation dI_T/dt. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation dI_T/dt.

Triacs logic level

BT134 series D

GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

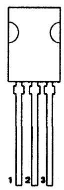
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BT134-	**500D**	**600D**	
V_{DRM}	Repetitive peak off-state voltages	500	600	V
$I_{T(RMS)}$	RMS on-state current	4	4	A
I_{TSM}	Non-repetitive peak on-state current	25	25	A

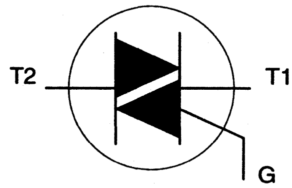
PINNING - SOT82

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
tab	main terminal 2

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX. -500	MAX. -600	UNIT
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 107$ ˚C	-	4		A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$				
		t = 20 ms	-	25		A
		t = 16.7 ms	-	27		A
I^2t	I^2t for fusing	t = 10 ms	-	3.1		A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 6$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs				
		T2+ G+	-	50		A/µs
		T2+ G-	-	50		A/µs
		T2- G-	-	50		A/µs
		T2- G+	-	10		A/µs
I_{GM}	Peak gate current		-	2		A
V_{GM}	Peak gate voltage		-	5		V
P_{GM}	Peak gate power		-	5		W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5		W
T_{stg}	Storage temperature		-40	150		˚C
T_j	Operating junction temperature		-	125		˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	full cycle	-	-	3.0	K/W
		half cycle	-	-	3.7	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	100	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	-	2.0	5	mA
		T2+ G-	-	2.5	5	mA
		T2- G-	-	2.5	5	mA
		T2- G+	-	5.0	10	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	1.6	10	mA
		T2+ G-	-	4.5	15	mA
		T2- G-	-	1.2	10	mA
		T2- G+	-	2.2	15	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	1.2	10	mA
V_T	On-state voltage	I_T = 5 A	-	1.4	1.70	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; R_{GK} = 1 kΩ	-	5	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 6 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs

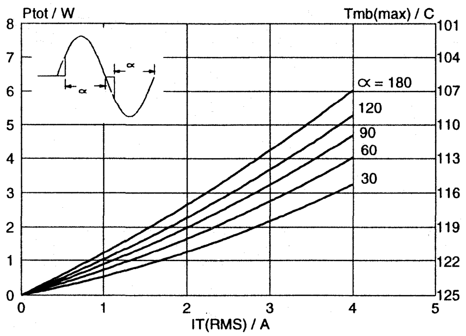


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

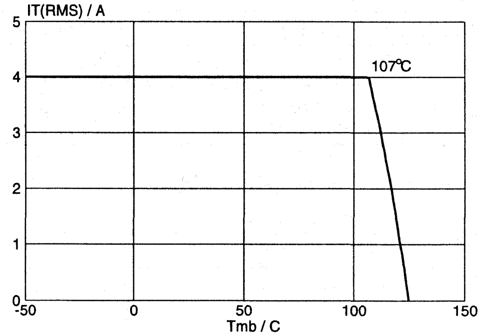


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

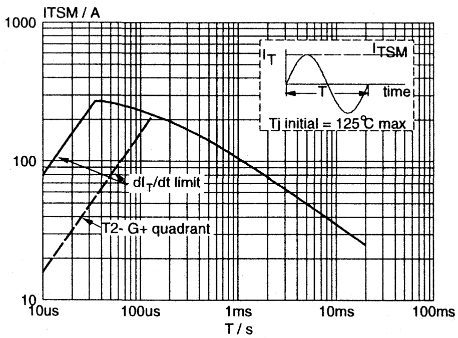


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

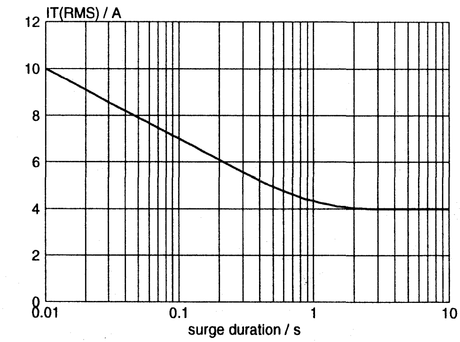


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 107$°C.

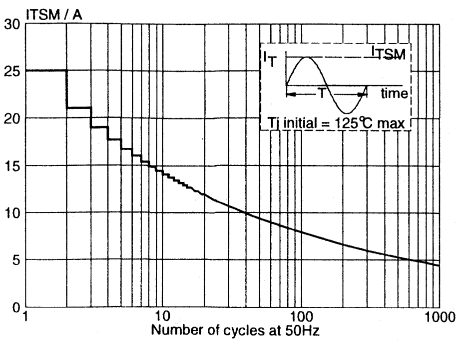


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

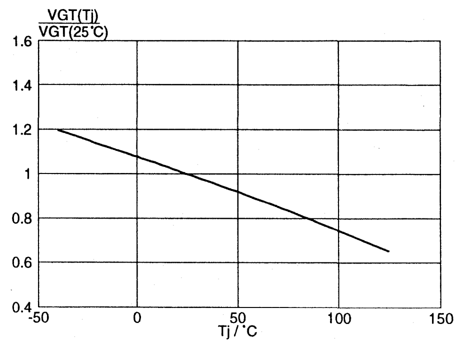


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25$°C), versus junction temperature T_j.

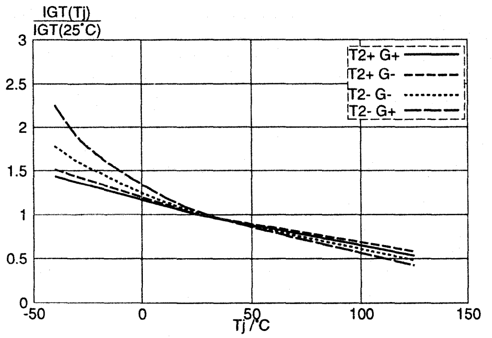


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/\ I_{GT}(25˚C)$, versus junction temperature T_j.

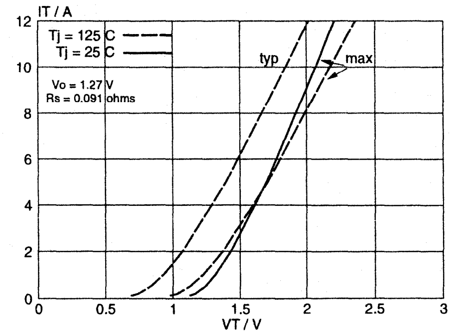


Fig.10. Typical and maximum on-state characteristic.

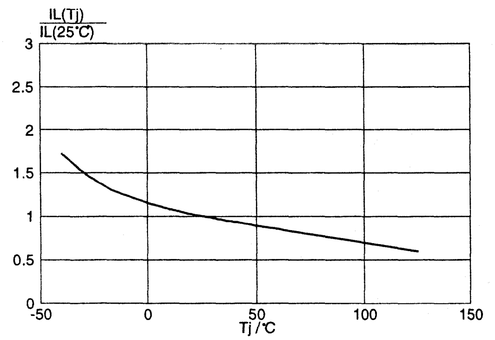


Fig.8. Normalised latching current $I_L(T_j)/\ I_L(25˚C)$, versus junction temperature T_j.

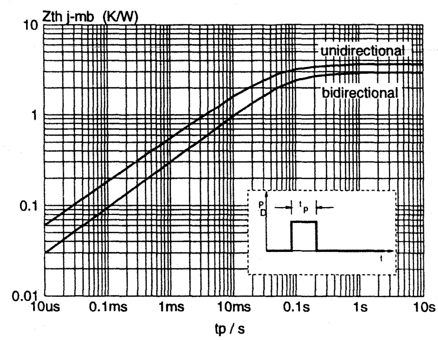


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width t_p.

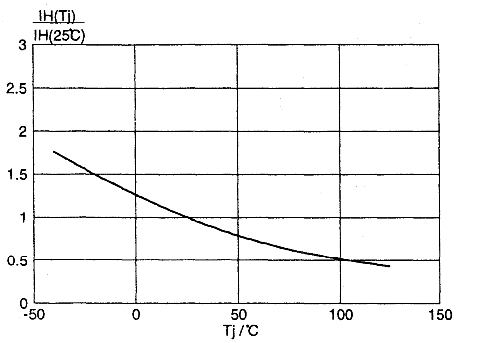


Fig.9. Normalised holding current $I_H(T_j)/\ I_H(25˚C)$, versus junction temperature T_j.

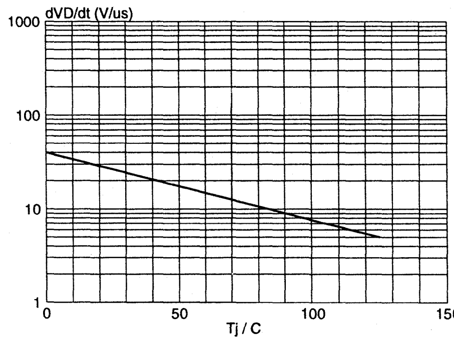


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

Triacs sensitive gate | BT134 series E

GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

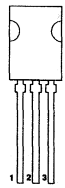
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT134-	500E	600E	800E	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	4	4	4	A
I_{TSM}	Non-repetitive peak on-state current	25	25	25	A

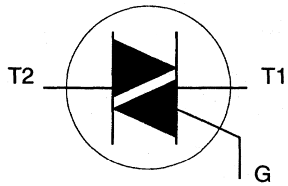
PINNING - SOT82

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
tab	main terminal 2

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	-600	-800	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 107$ ˚C	-	4			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 20 ms	-	25			A
		t = 16.7 ms	-	27			A
I^2t	I^2t for fusing	t = 10 ms	-	3.1			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 6$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs					
		T2+ G+	-	50			A/µs
		T2+ G-	-	50			A/µs
		T2- G-	-	50			A/µs
		T2- G+	-	10			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base	full cycle	-	-	3.0	K/W
		half cycle	-	-	3.7	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	in free air	-	100	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	-	2.5	10	mA
		T2+ G-	-	4.0	10	mA
		T2- G-	-	5.0	10	mA
		T2- G+	-	11	25	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	3.0	15	mA
		T2+ G-	-	10	20	mA
		T2- G-	-	2.5	15	mA
		T2- G+	-	4.0	20	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	2.2	15	mA
V_T	On-state voltage	I_T = 5 A	-	1.4	1.70	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	$V_D = V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	-	50	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 6 A; $V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs

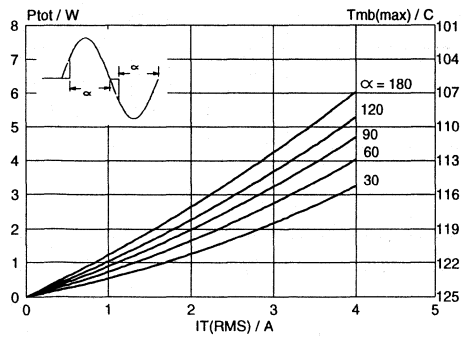


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

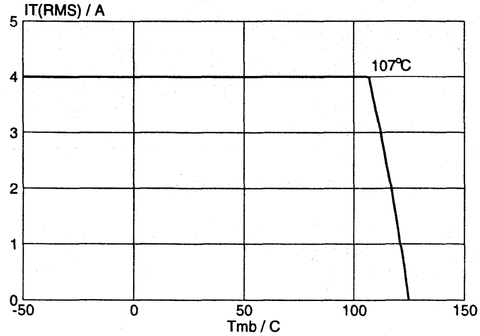


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

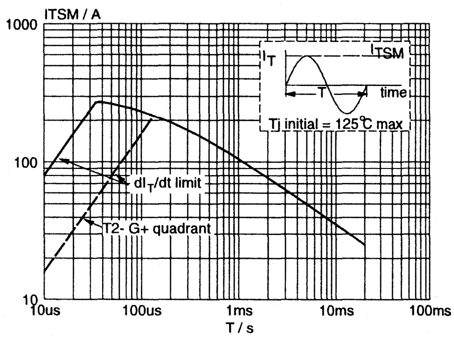


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq$ 20ms.

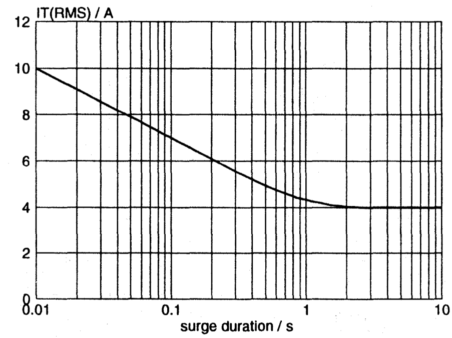


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq$ 107˚C.

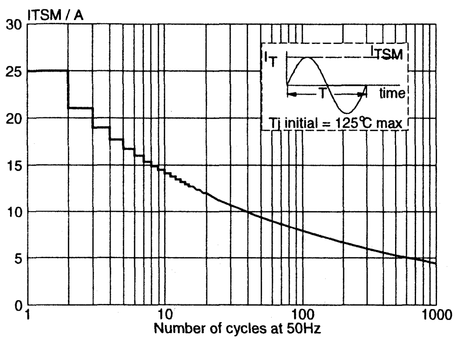


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

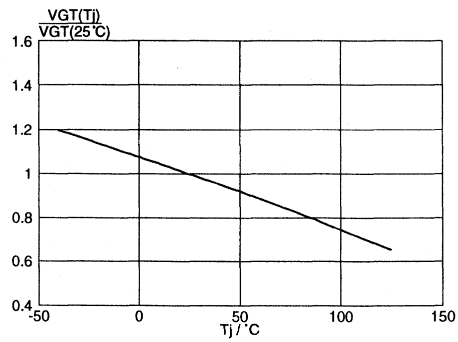


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25˚C)$, versus junction temperature T_j.

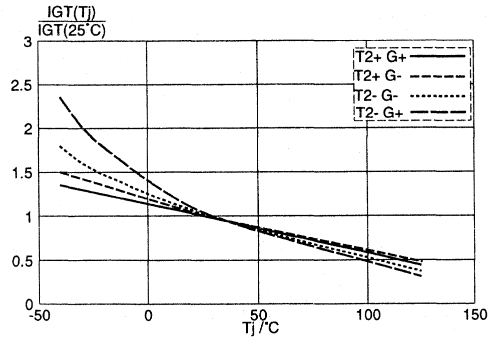


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/I_{GT}(25˚C)$, versus junction temperature T_j.

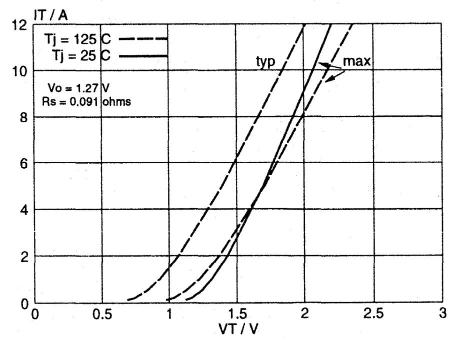


Fig.10. Typical and maximum on-state characteristic.

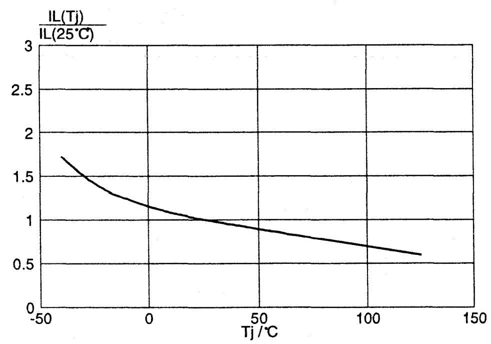


Fig.8. Normalised latching current $I_L(T_j)/I_L(25˚C)$, versus junction temperature T_j.

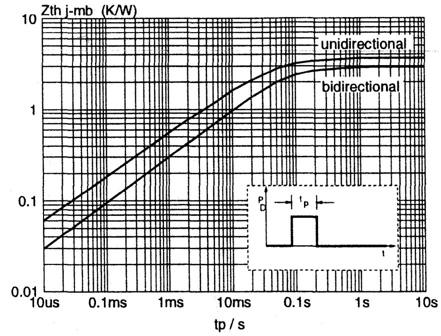


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width t_p.

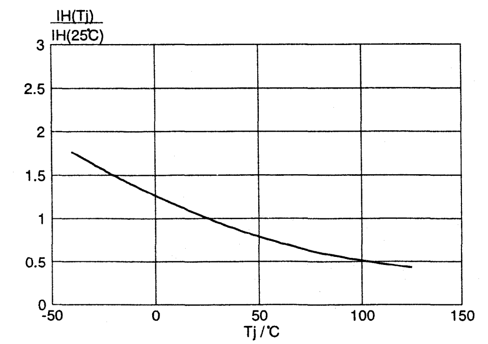


Fig.9. Normalised holding current $I_H(T_j)/I_H(25˚C)$, versus junction temperature T_j.

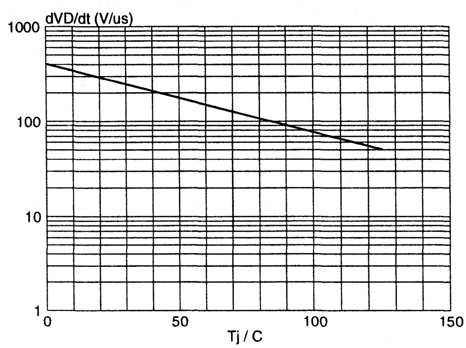


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

GENERAL DESCRIPTION

Glass passivated triacs in a plastic envelope suitable for surface mounting, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

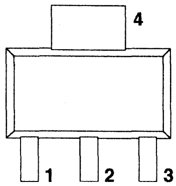
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT134W-	**500**	**600**	**800**	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	1	1	1	A
I_{TSM}	Non-repetitive peak on-state current	10	10	10	A

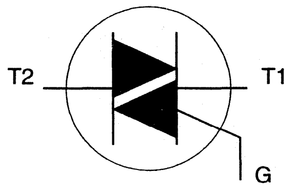
PINNING - SOT223

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
tab	main terminal 2

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	**-600**	**-800**	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{sp} \leq 108$ ˚C	-	1			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 20 ms	-	10			A
		t = 16.7 ms	-	11			A
I^2t	I^2t for fusing	t = 10 ms	-	0.5			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 1.5$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs					
		T2+ G+	-	50			A/µs
		T2+ G-	-	50			A/µs
		T2- G-	-	50			A/µs
		T2- G+	-	10			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-sp}$	Thermal resistance junction to solder point	full or half cycle	-	-	15	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	pcb mounted; minimum footprint	-	156	-	K/W
		pcb mounted; pad area as in fig:14	-	70	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	-	5	35	mA
		T2+ G-	-	8	35	mA
		T2- G-	-	11	35	mA
		T2- G+	-	30	70	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	7	20	mA
		T2+ G-	-	16	30	mA
		T2- G-	-	5	20	mA
		T2- G+	-	7	30	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	5	15	mA
V_T	On-state voltage	I_T = 2 A	-	1.2	1.5	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	$V_D = V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	100	250	-	V/µs
dV_{com}/dt	Critical rate of change of commutating voltage	V_{DM} = 400 V; T_j = 95 ˚C; $I_{T(RMS)}$ = 1 A; dI_{com}/dt = 1.8 A/ms; gate open circuit	10	50	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 1.5 A; $V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs

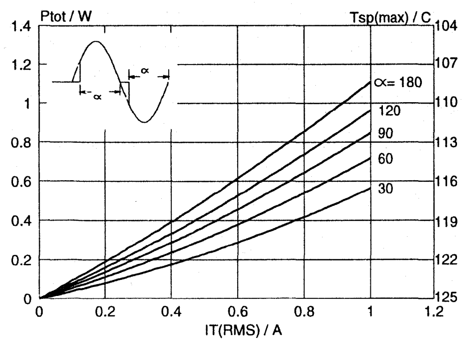


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

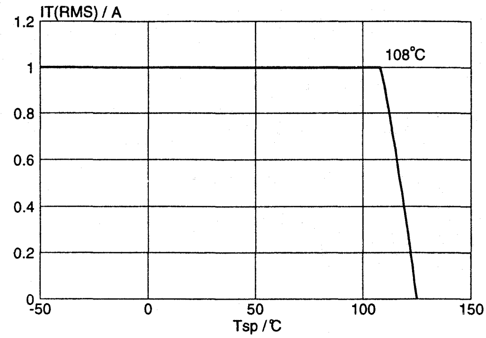


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus solder point temperature T_{sp}.

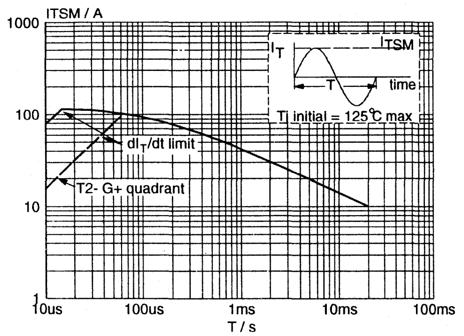


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

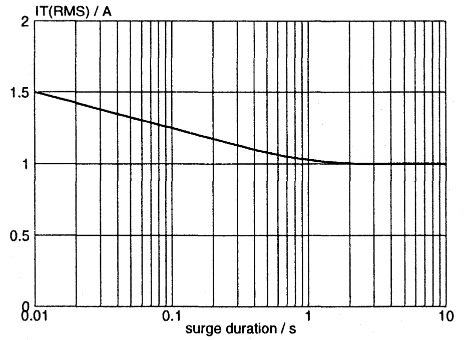


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{sp} \leq 108°C$.

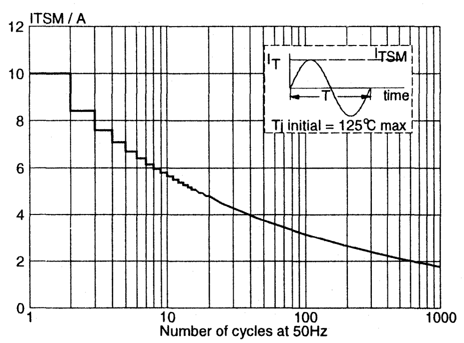


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

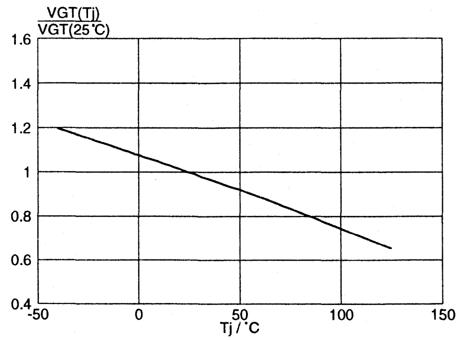


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature T_j.

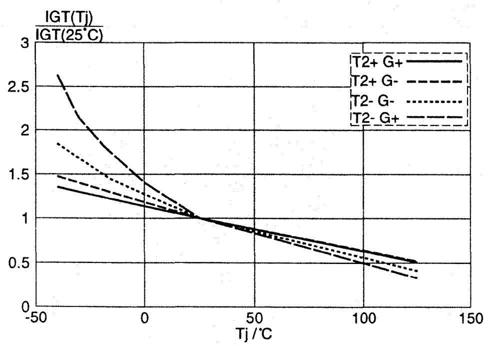


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

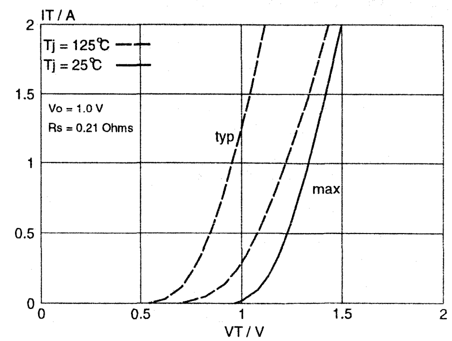


Fig.10. Typical and maximum on-state characteristic.

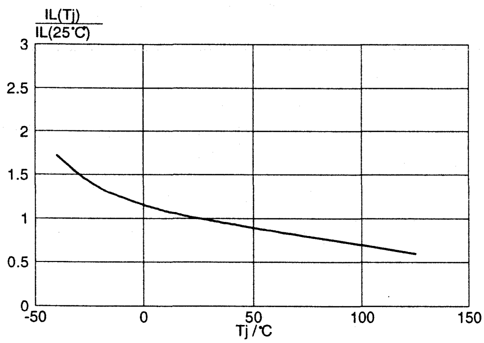


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.

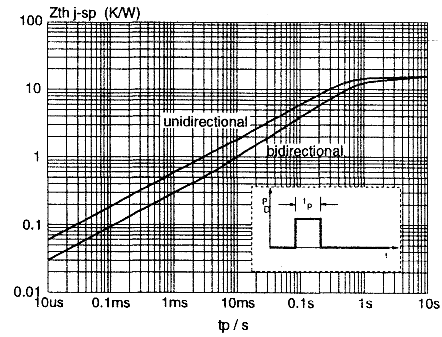


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}sp}$, versus pulse width t_p.

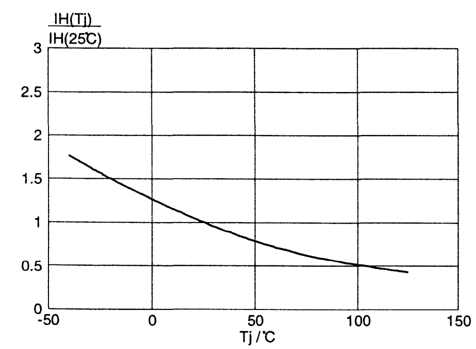


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j.

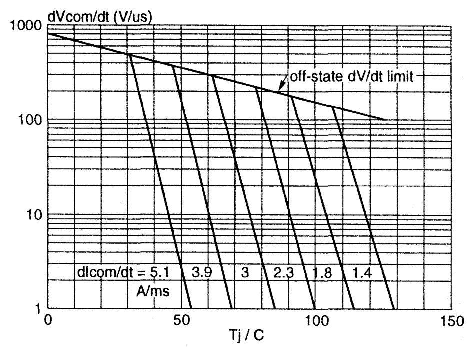


Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation dI_T/dt. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation dI_T/dt.

MOUNTING INSTRUCTIONS

Dimensions in mm.

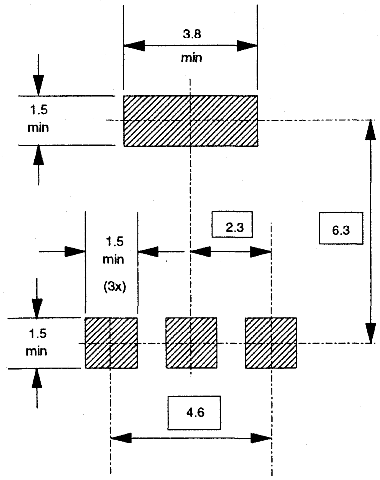


Fig.13. soldering pattern for surface mounting SOT223.

PRINTED CIRCUIT BOARD

Dimensions in mm.

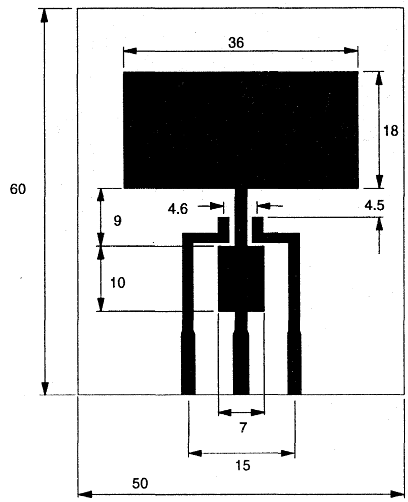


Fig.14. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 µm thick).

Triacs logic level

BT134W series D

GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope suitable for surface mounting, intended for use in general purpose bidirectional switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

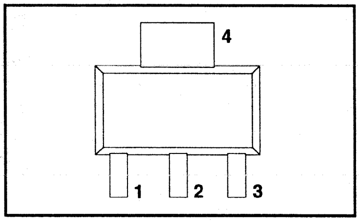
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BT134W-	500D	600D	
V_{DRM}	Repetitive peak off-state voltages	500	600	V
$I_{T(RMS)}$	RMS on-state current	1	1	A
I_{TSM}	Non-repetitive peak on-state current	10	10	A

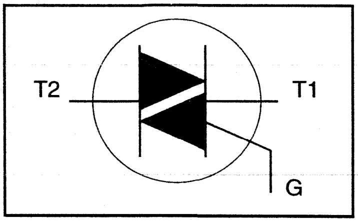
PINNING - SOT223

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
tab	main terminal 2

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
				-500	-600	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{sp} \leq 108$ ˚C	-	1		A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$				
		t = 20 ms	-	10		A
		t = 16.7 ms	-	11		A
I^2t	I^2t for fusing	t = 10 ms	-	0.5		A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 1.5$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs				
		T2+ G+	-	50		A/µs
		T2+ G-	-	50		A/µs
		T2- G-	-	50		A/µs
		T2- G+	-	10		A/µs
I_{GM}	Peak gate current		-	2		A
V_{GM}	Peak gate voltage		-	5		V
P_{GM}	Peak gate power		-	5		W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5		W
T_{stg}	Storage temperature		-40	150		˚C
T_j	Operating junction temperature		-	125		˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}sp}$	Thermal resistance junction to solder point	full or half cycle	-	-	15	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	pcb mounted; minimum footprint	-	156	-	K/W
		pcb mounted; pad area as in fig:14	-	70	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	-	2.0	5	mA
		T2+ G-	-	2.5	5	mA
		T2- G-	-	2.5	5	mA
		T2- G+	-	5.0	10	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	1.6	10	mA
		T2+ G-	-	4.5	15	mA
		T2- G-	-	1.2	10	mA
		T2- G+	-	2.2	15	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	1.2	10	mA
V_T	On-state voltage	I_T = 2 A	-	1.2	1.5	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	$V_D = V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of change of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; R_{GK} = 1 kΩ	-	5	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 1.5 A; $V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs

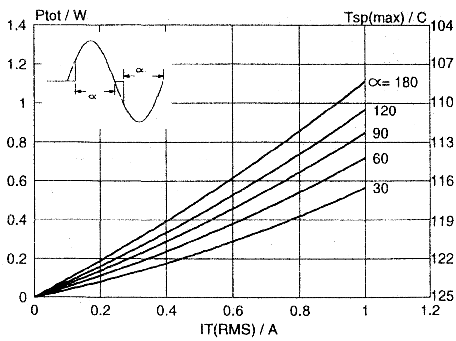


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

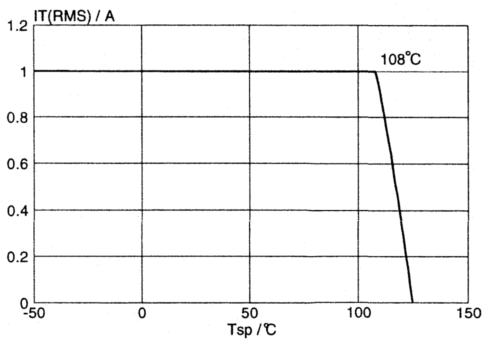


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus solder point temperature T_{sp}.

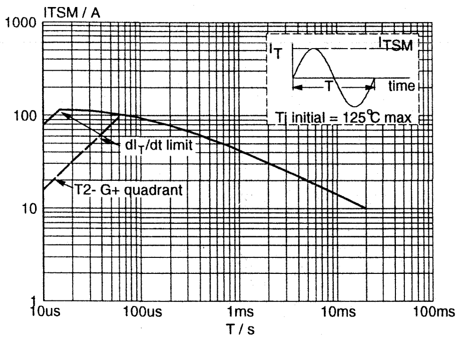


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

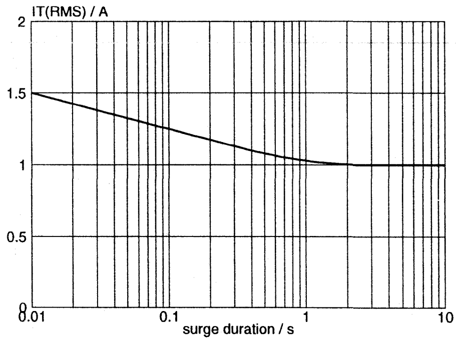


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{sp} \leq 108$˚C.

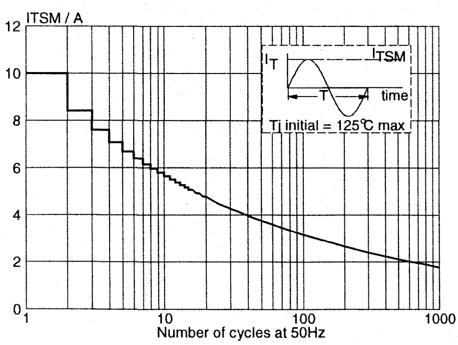


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

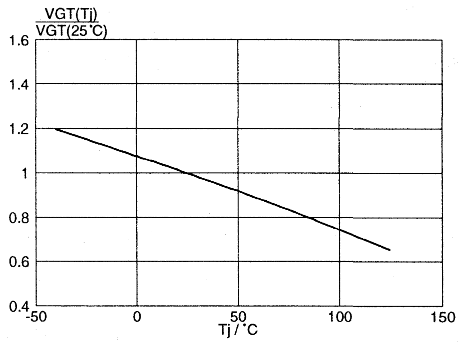


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)$/ V_{GT}(25˚C), versus junction temperature T_j.

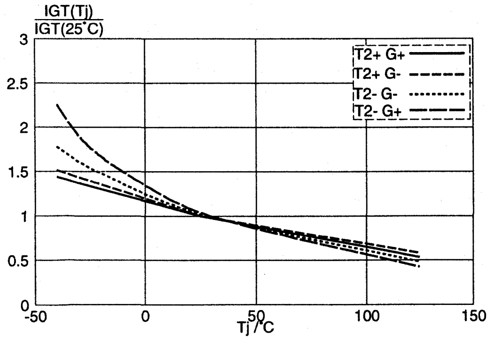


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

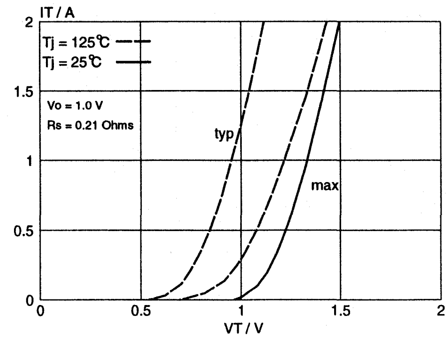


Fig.10. Typical and maximum on-state characteristic.

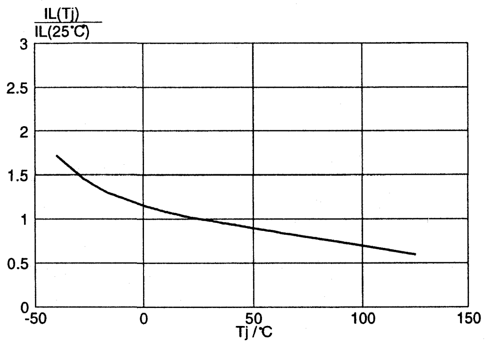


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.

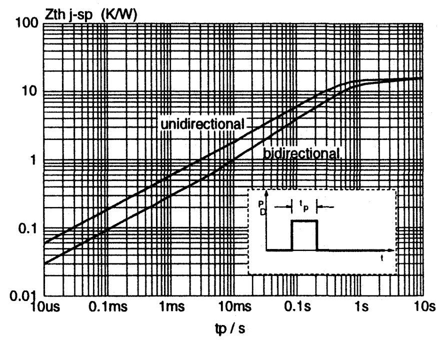


Fig.11. Transient thermal impedance $Z_{th\,j\text{-}sp}$, versus pulse width t_p.

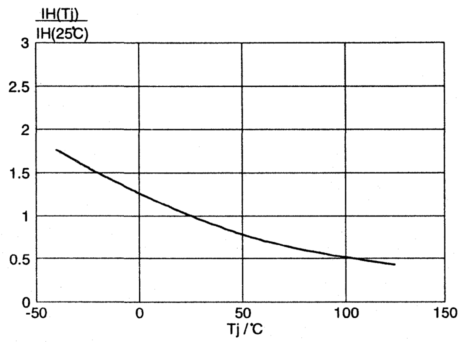


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j.

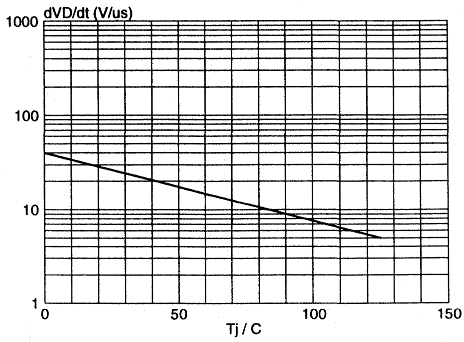


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

MOUNTING INSTRUCTIONS

Dimensions in mm.

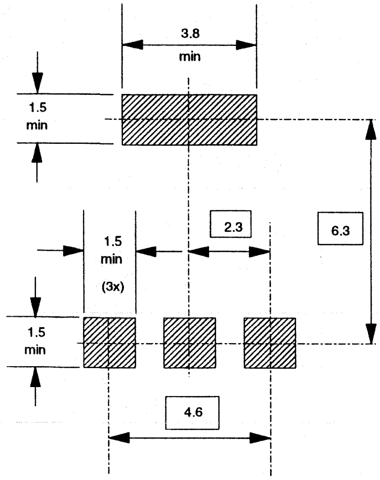


Fig.13. soldering pattern for surface mounting SOT223.

PRINTED CIRCUIT BOARD

Dimensions in mm.

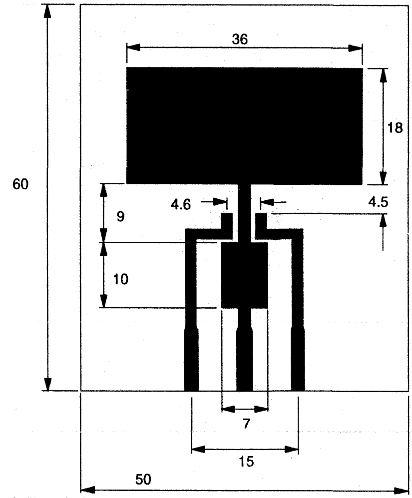


Fig.14. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 µm thick).

Triacs sensitive gate

BT134W series E

GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope suitable for surface mounting, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

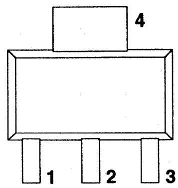
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BT134W-	500E	600E	
V_{DRM}	Repetitive peak off-state voltages	500	600	V
$I_{T(RMS)}$	RMS on-state current	1	1	A
I_{TSM}	Non-repetitive peak on-state current	10	10	A

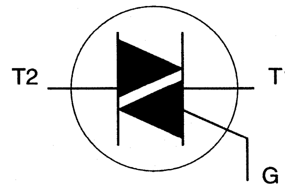
PINNING - SOT223

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
tab	main terminal 2

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
				-500	-600	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{sp} \leq 108$ ˚C	-	1		A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$				
		t = 20 ms	-	10		A
		t = 16.7 ms	-	11		A
I^2t	I^2t for fusing	t = 10 ms	-	0.5		A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 1.5$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs				
		T2+ G+	-	50		A/µs
		T2+ G-	-	50		A/µs
		T2- G-	-	50		A/µs
		T2- G+	-	10		A/µs
I_{GM}	Peak gate current		-	2		A
V_{GM}	Peak gate voltage		-	5		V
P_{GM}	Peak gate power		-	5		W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5		W
T_{stg}	Storage temperature		-40	150		˚C
T_j	Operating junction temperature		-	125		˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}sp}$	Thermal resistance junction to solder point	full or half cycle	-	-	15	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	pcb mounted; minimum footprint	-	156	-	K/W
		pcb mounted; pad area as in fig:14	-	70	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	-	2.5	10	mA
		T2+ G-	-	4.0	10	mA
		T2- G-	-	5.0	10	mA
		T2- G+	-	11	25	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	3.0	15	mA
		T2+ G-	-	10	20	mA
		T2- G-	-	2.5	15	mA
		T2- G+	-	4.0	20	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	2.2	15	mA
V_T	On-state voltage	I_T = 2 A	-	1.2	1.5	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	$V_D = V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	-	30	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 1.5 A; $V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs

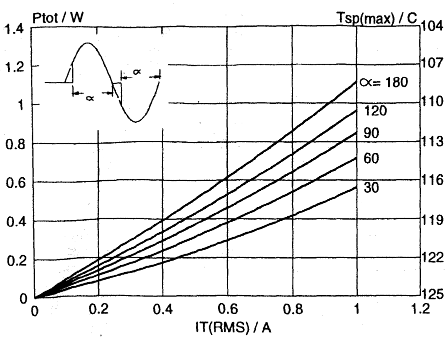


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

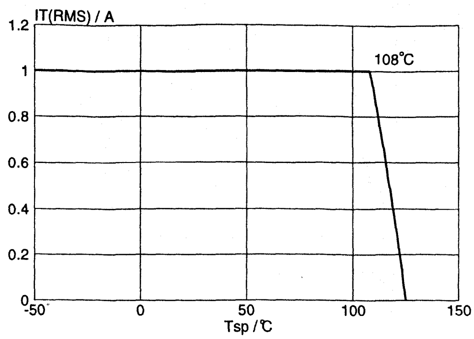


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus solder point temperature T_{sp}.

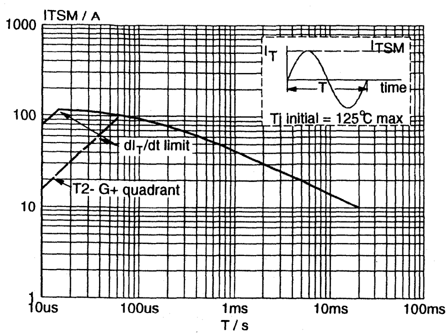


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

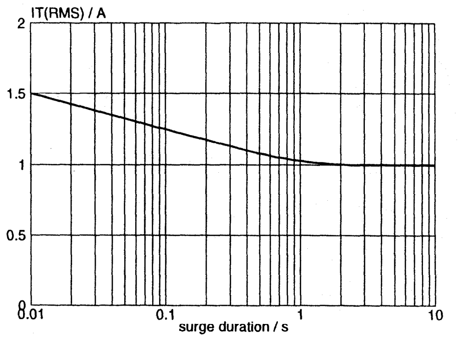


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{sp} \leq 108$°C.

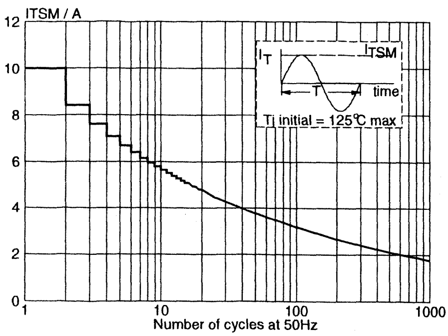


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

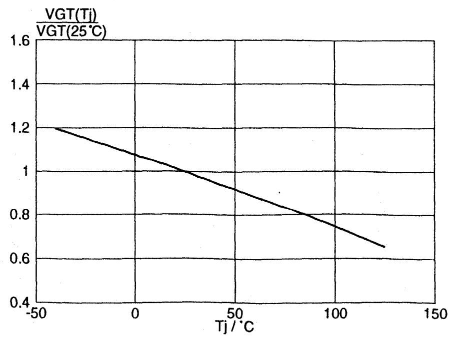


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25°C)$, versus junction temperature T_j.

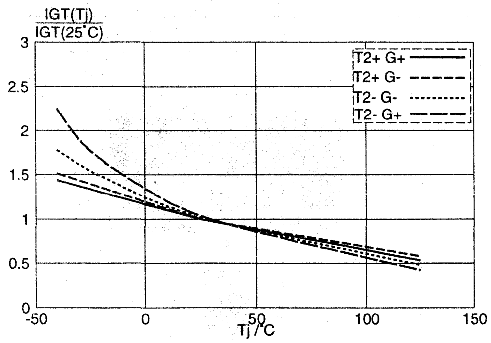


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/I_{GT}(25˚C)$, versus junction temperature T_j.

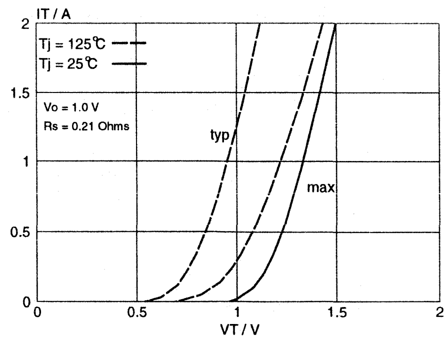


Fig.10. Typical and maximum on-state characteristic.

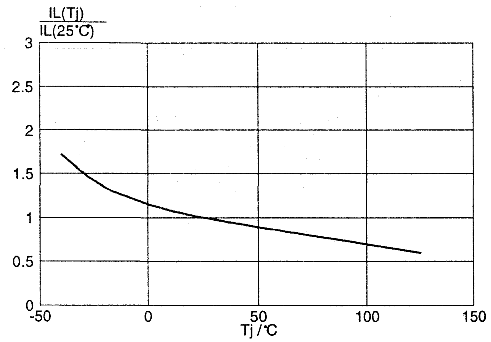


Fig.8. Normalised latching current $I_L(T_j)/I_L(25˚C)$, versus junction temperature T_j.

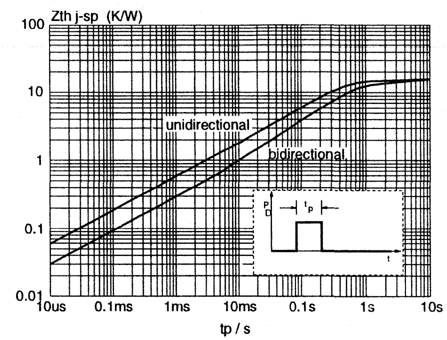


Fig.11. Transient thermal impedance $Z_{th\,j\text{-}sp}$, versus pulse width t_p.

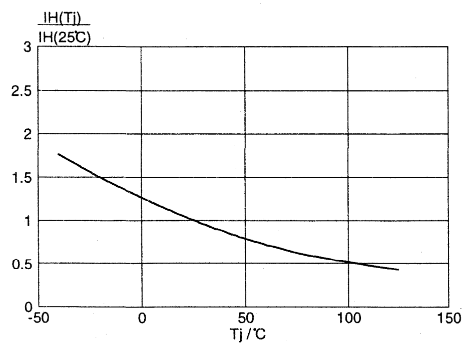


Fig.9. Normalised holding current $I_H(T_j)/I_H(25˚C)$, versus junction temperature T_j.

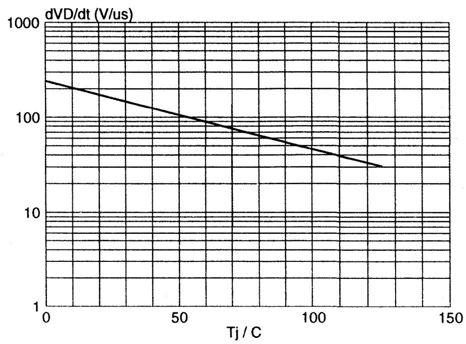


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

MOUNTING INSTRUCTIONS

Dimensions in mm.

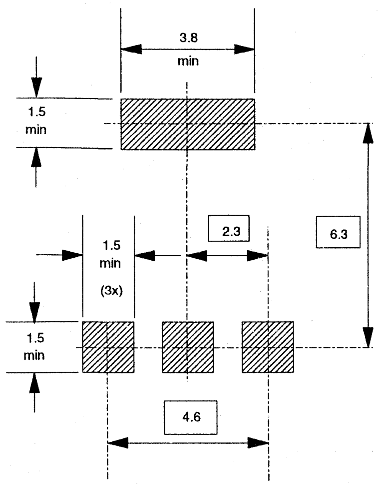


Fig.13. soldering pattern for surface mounting SOT223.

PRINTED CIRCUIT BOARD

Dimensions in mm.

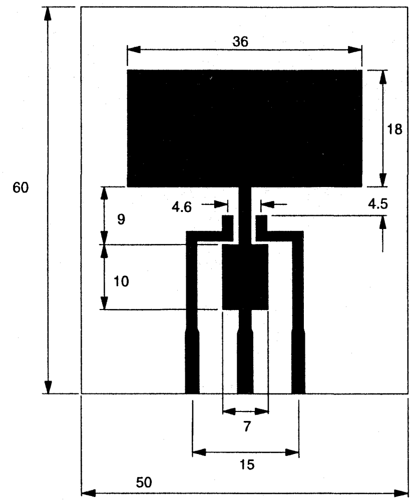


Fig.14. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 µm thick).

GENERAL DESCRIPTION

Glass passivated triacs in a plastic envelope, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

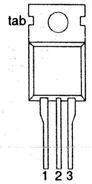
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT136-	500	600	800	
	BT136-	500F	600F	800F	
	BT136-	500G	600G	800G	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	4	4	4	A
I_{TSM}	Non-repetitive peak on-state current	25	25	25	A

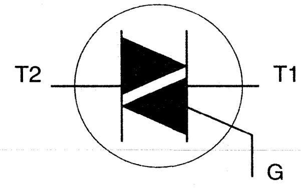
PINNING - TO220AB

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
tab	main terminal 2

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	-600	-800	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 107$ ˚C	-	4			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 20 ms	-	25			A
		t = 16.7 ms	-	27			A
I^2t	I^2t for fusing	t = 10 ms	-	3.1			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 6$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs					
		T2+ G+	-	50			A/µs
		T2+ G-	-	50			A/µs
		T2- G-	-	50			A/µs
		T2- G+	-	10			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	full cycle	-	-	3.0	K/W
		half cycle	-	-	3.7	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.			UNIT
		BT136-			...	...F	...G	
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A						
		T2+ G+	-	5	35	25	50	mA
		T2+ G-	-	8	35	25	50	mA
		T2- G-	-	11	35	25	50	mA
		T2- G+	-	30	70	70	100	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A						
		T2+ G+	-	7	20	20	30	mA
		T2+ G-	-	16	30	30	45	mA
		T2- G-	-	5	20	20	30	mA
		T2- G+	-	7	30	30	45	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	5	15	15	30	mA
V_T	On-state voltage	I_T = 5 A	-	1.4	1.70			V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5			V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-			V
I_D	Off-state leakage current	$V_D = V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5			mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.			TYP.	MAX.	UNIT
		BT136-	...	...F	...G			
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	100	50	200	250	-	V/µs
dV_{com}/dt	Critical rate of change of commutating voltage	V_{DM} = 400 V; T_j = 95 ˚C; $I_{T(RMS)}$ = 4 A; dI_{com}/dt = 1.8 A/ms; gate open circuit	-	-	10	50	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 6 A; $V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	-	-	2	-	µs

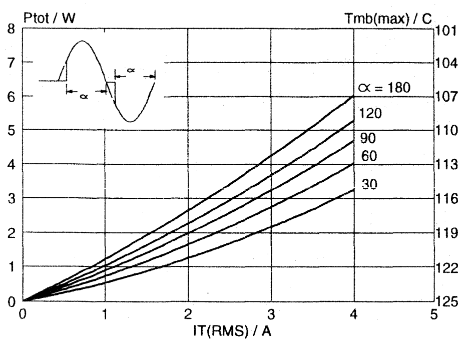


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

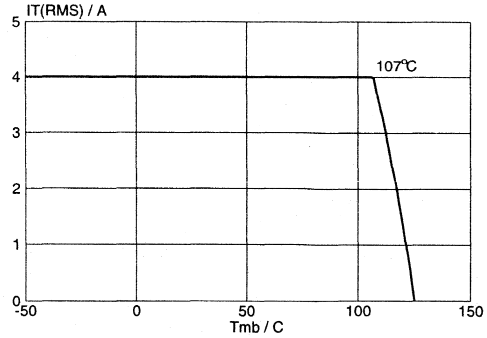


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

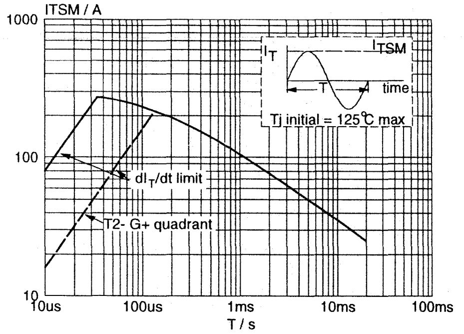


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

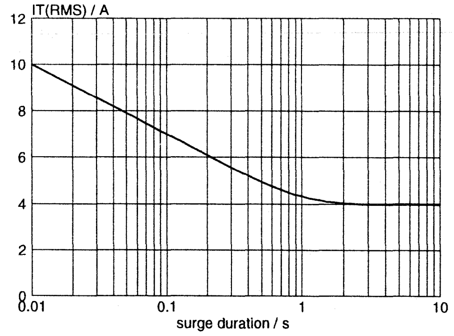


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 107˚C$.

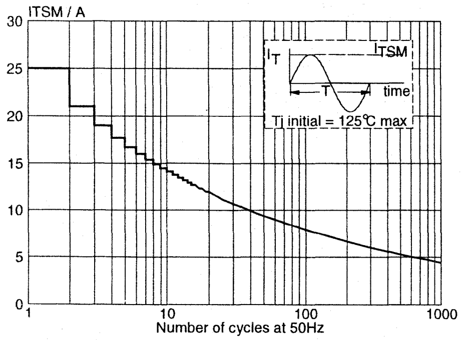


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

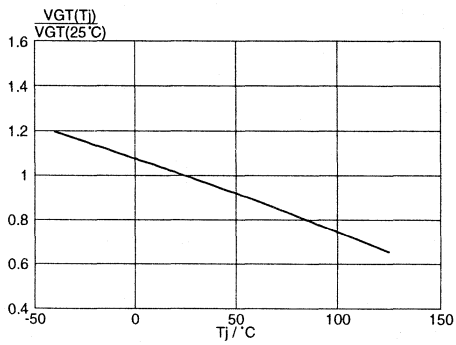


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25˚C)$, versus junction temperature T_j.

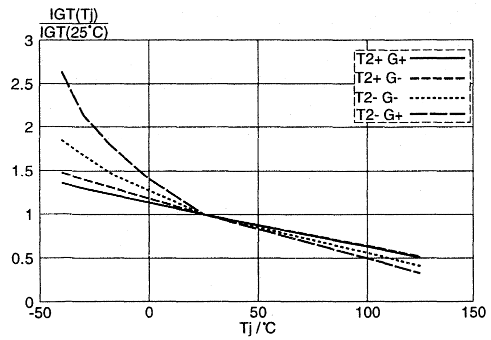


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/I_{GT}(25˚C)$, versus junction temperature T_j.

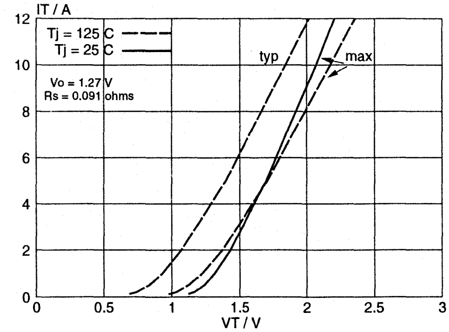


Fig.10. Typical and maximum on-state characteristic.

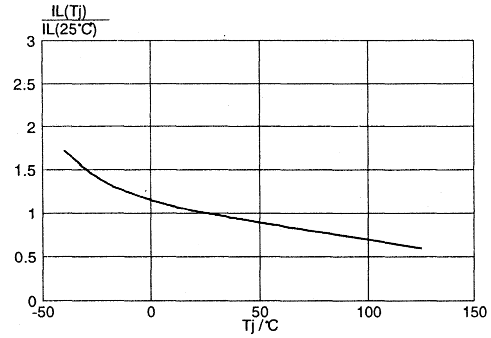


Fig.8. Normalised latching current $I_L(T_j)/I_L(25˚C)$, versus junction temperature T_j.

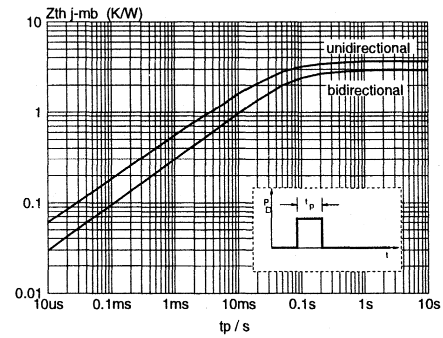


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width t_p.

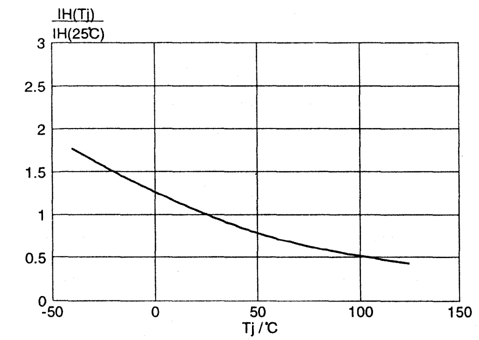


Fig.9. Normalised holding current $I_H(T_j)/I_H(25˚C)$, versus junction temperature T_j.

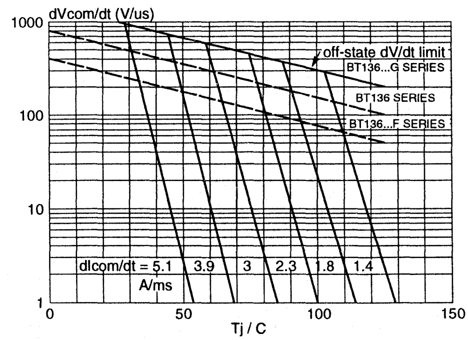


Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation dI_T/dt. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation dI_T/dt.

Triacs logic level

BT136 series D

GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

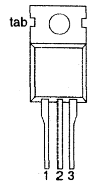
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BT136-	500D	600D	
V_{DRM}	Repetitive peak off-state voltages	500	600	V
$I_{T(RMS)}$	RMS on-state current	4	4	A
I_{TSM}	Non-repetitive peak on-state current	25	25	A

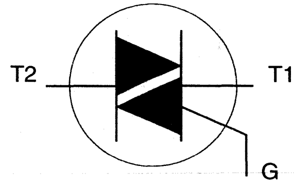
PINNING - TO220AB

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
tab	main terminal 2

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
				-500	-600	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 107$ ˚C	-	4		A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$				
		t = 20 ms	-	25		A
		t = 16.7 ms	-	27		A
I^2t	I^2t for fusing	t = 10 ms	-	3.1		A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 6$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs				
		T2+ G+	-	50		A/µs
		T2+ G-	-	50		A/µs
		T2- G-	-	50		A/µs
		T2- G+	-	10		A/µs
I_{GM}	Peak gate current		-	2		A
V_{GM}	Peak gate voltage		-	5		V
P_{GM}	Peak gate power		-	5		W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5		W
T_{stg}	Storage temperature		-40	150		˚C
T_j	Operating junction temperature		-	125		˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base	full cycle half cycle	- -	- -	3.0 3.7	K/W K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	-	2.0	5	mA
		T2+ G-	-	2.5	5	mA
		T2- G-	-	2.5	5	mA
		T2- G+	-	5.0	10	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	1.6	10	mA
		T2+ G-	-	4.5	15	mA
		T2- G-	-	1.2	10	mA
		T2- G+	-	2.2	15	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	1.2	10	mA
V_T	On-state voltage	I_T = 5 A	-	1.4	1.70	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	$V_D = V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; R_{GK} = 1 kΩ	-	5	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 6 A; $V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs

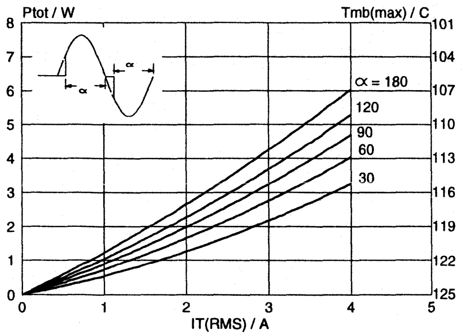


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

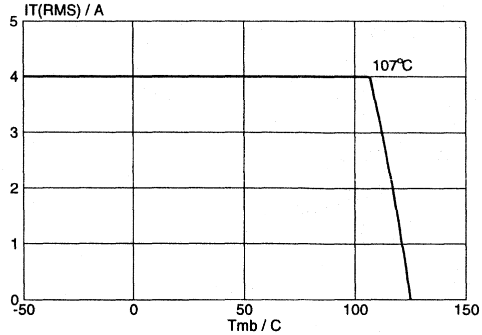


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

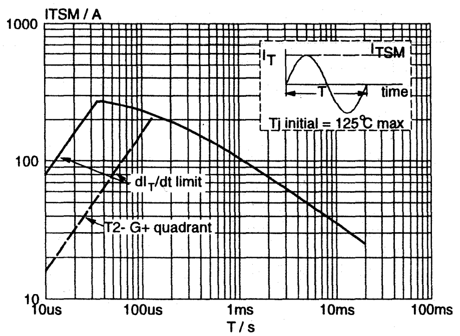


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

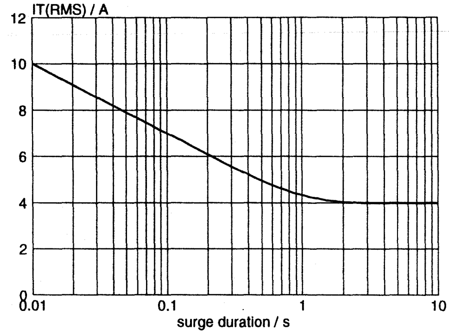


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 107^{\circ}C$.

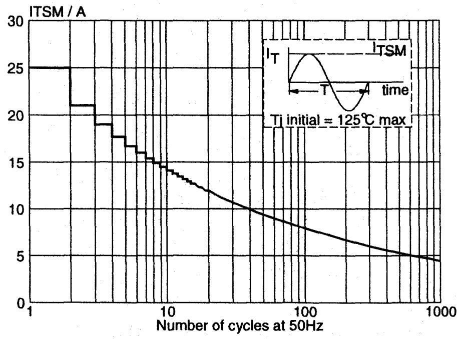


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

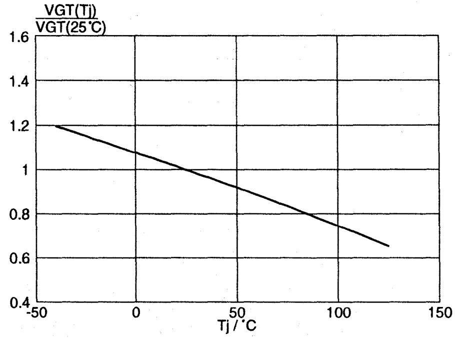


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25^{\circ}C)$, versus junction temperature T_j.

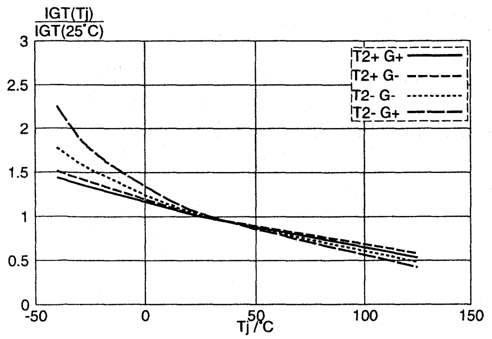


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25^{\circ}C)$, versus junction temperature T_j.

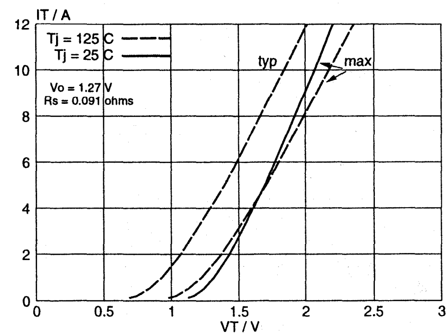


Fig.10. Typical and maximum on-state characteristic.

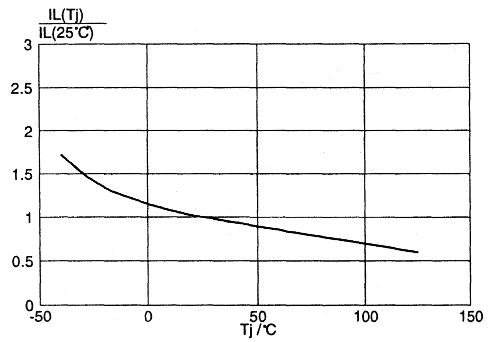


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25^{\circ}C)$, versus junction temperature T_j.

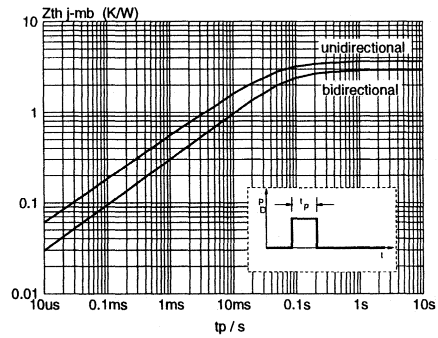


Fig.11. Transient thermal impedance $Z_{th\ j-mb}$, versus pulse width t_p.

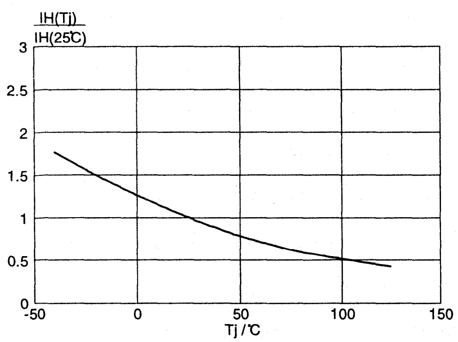


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25^{\circ}C)$, versus junction temperature T_j.

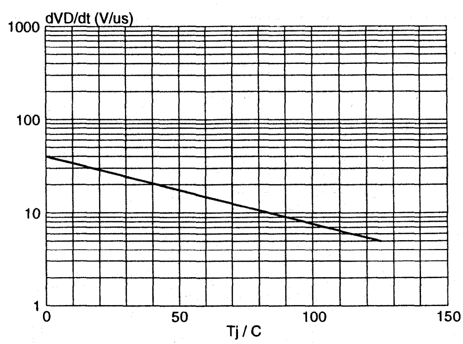


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

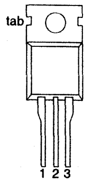
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT136-	500E	600E	800E	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	4	4	4	A
I_{TSM}	Non-repetitive peak on-state current	25	25	25	A

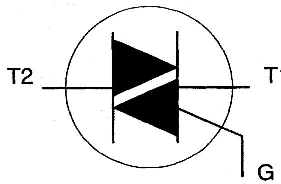
PINNING - TO220AB

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
tab	main terminal 2

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	-600	-800	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 107$ ˚C	-	4			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 20 ms	-	25			A
		t = 16.7 ms	-	27			A
I^2t	I^2t for fusing	t = 10 ms	-	3.1			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 6$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/μs					
		T2+ G+	-	50			A/μs
		T2+ G-	-	50			A/μs
		T2- G-	-	50			A/μs
		T2- G+	-	10			A/μs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/μs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	full cycle	-	-	3.0	K/W
		half cycle	-	-	3.7	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	-	2.5	10	mA
		T2+ G-	-	4.0	10	mA
		T2- G-	-	5.0	10	mA
		T2- G+	-	11	25	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	3.0	15	mA
		T2+ G-	-	10	20	mA
		T2- G-	-	2.5	15	mA
		T2- G+	-	4.0	20	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	2.2	15	mA
V_T	On-state voltage	I_T = 5 A	-	1.4	1.70	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	-	50	-	V/μs
t_{gt}	Gate controlled turn-on time	I_{TM} = 6 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/μs	-	2	-	μs

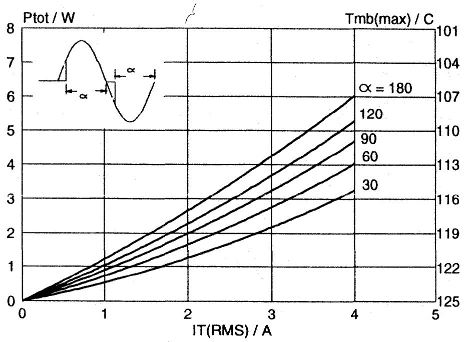


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

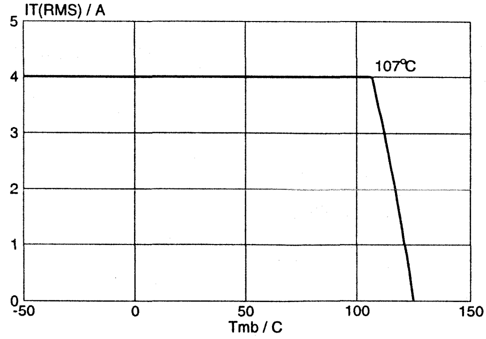


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

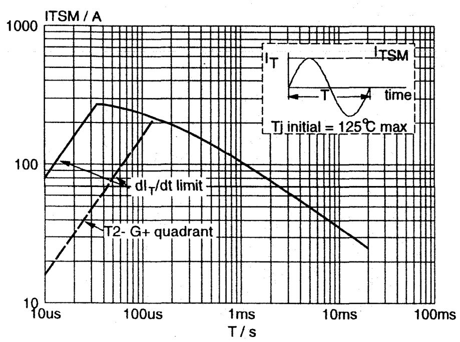


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq$ 20ms.

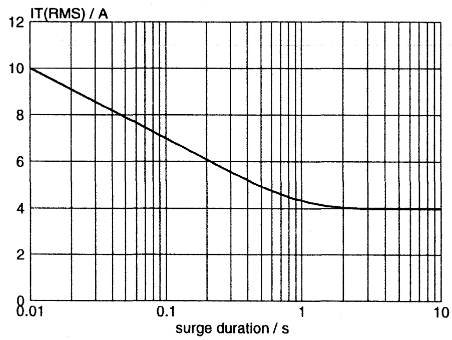


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq$ 107°C.

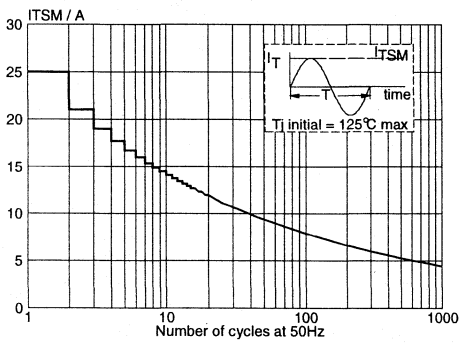


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

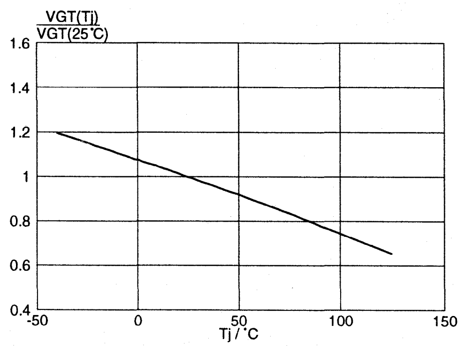


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)$/ V_{GT}(25°C), versus junction temperature T_j.

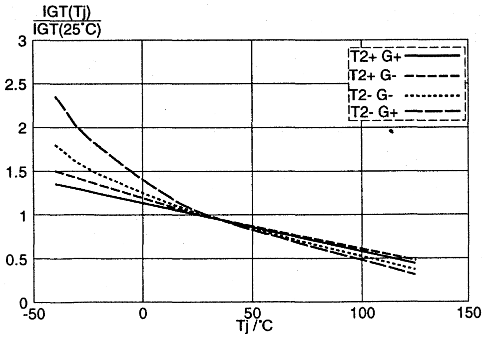


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/I_{GT}(25˚C)$, versus junction temperature T_j.

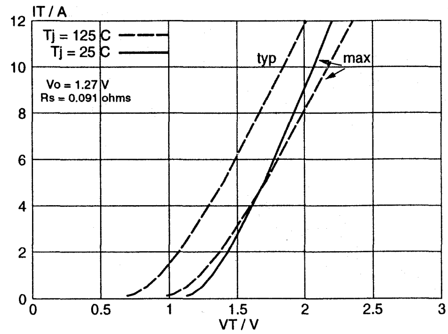


Fig.10. Typical and maximum on-state characteristic.

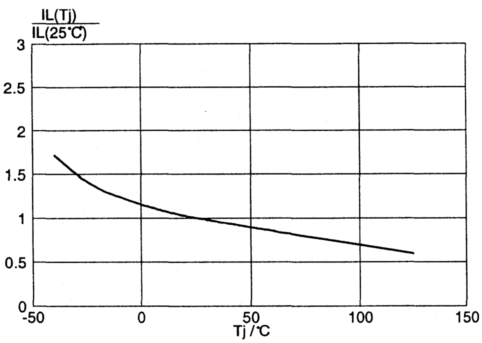


Fig.8. Normalised latching current $I_L(T_j)/I_L(25˚C)$, versus junction temperature T_j.

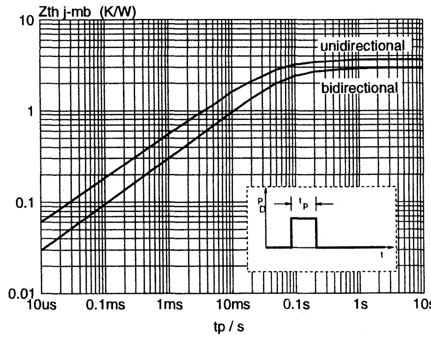


Fig.11. Transient thermal impedance $Z_{th\,j\text{-}mb}$, versus pulse width t_p.

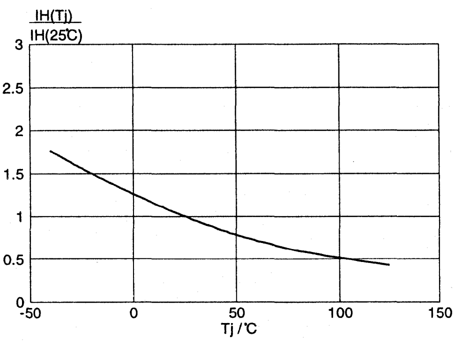


Fig.9. Normalised holding current $I_H(T_j)/I_H(25˚C)$, versus junction temperature T_j.

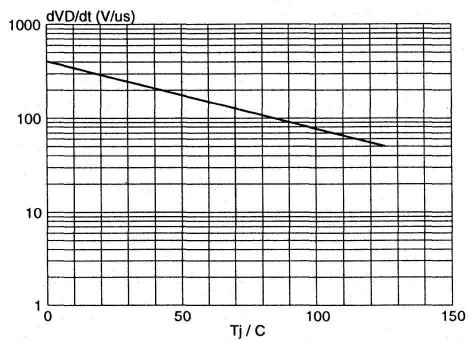


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

GENERAL DESCRIPTION

Glass passivated triacs in a full pack plastic envelope, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

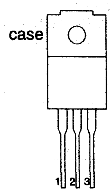
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT136F-	**500**	**600**	**800**	
	BT136F-	**500F**	**600F**	**800F**	
	BT136F-	**500G**	**600G**	**800G**	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	4	4	4	A
I_{TSM}	Non-repetitive peak on-state current	25	25	25	A

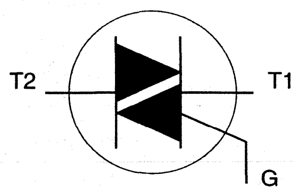
PINNING - SOT186

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	**-600**	**-800**	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{hs} \leq 92$ ˚C	-	4			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 20 ms	-	25			A
		t = 16.7 ms	-	27			A
I^2t	I^2t for fusing	t = 10 ms	-	3.1			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 6$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs					
		T2+ G+	-	50			A/µs
		T2+ G-	-	50			A/µs
		T2- G-	-	50			A/µs
		T2- G+	-	10			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	full or half cycle				
		with heatsink compound	-	-	5.5	K/W
		without heatsink compound	-	-	7.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.			UNIT
		BT136F-			...	...F	...G	
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A						
		T2+ G+	-	5	35	25	50	mA
		T2+ G-	-	8	35	25	50	mA
		T2- G-	-	11	35	25	50	mA
		T2- G+	-	30	70	70	100	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A						
		T2+ G+	-	7	20	20	30	mA
		T2+ G-	-	16	30	30	45	mA
		T2- G-	-	5	20	20	30	mA
		T2- G+	-	7	30	30	45	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	5	15	15	30	mA
V_T	On-state voltage	I_T = 5 A	-	1.4	1.70			V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5			V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-			V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5			mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.			TYP.	MAX.	UNIT
		BT136F-	...	...F	...G			
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$V; T_j = 125 ˚C; exponential waveform; gate open circuit	100	50	200	250	-	V/μs
dV_{com}/dt	Critical rate of change of commutating voltage	V_{DM} = 400 V; T_j = 95 ˚C; $I_{T(RMS)}$ = 4 A; dI_{com}/dt = 1.8 A/ms; gate open circuit	-	-	10	50	-	V/μs
t_{gt}	Gate controlled turn-on time	I_{TM} = 6 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/μs	-	-	-	2	-	μs

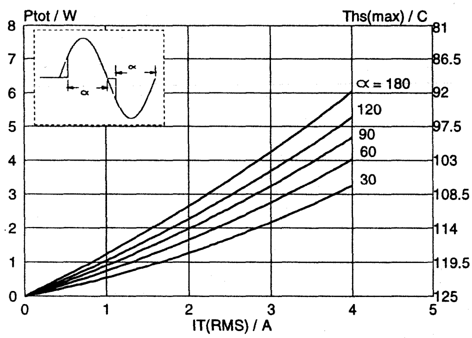


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

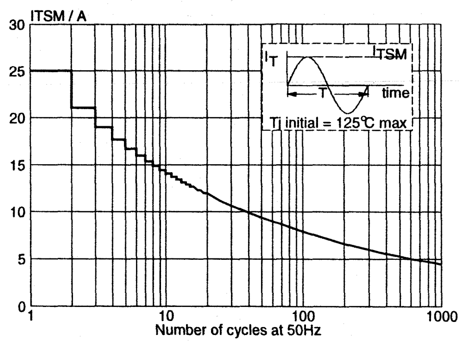


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

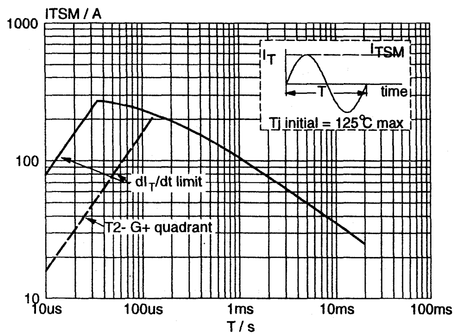


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq$ 20ms.

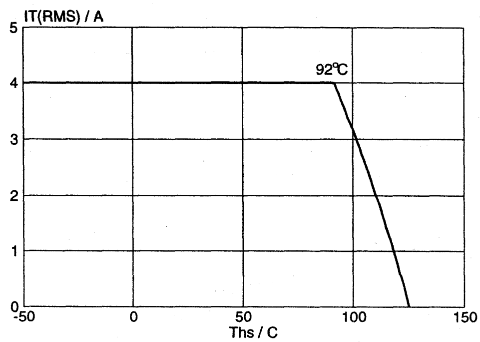


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature T_{hs}.

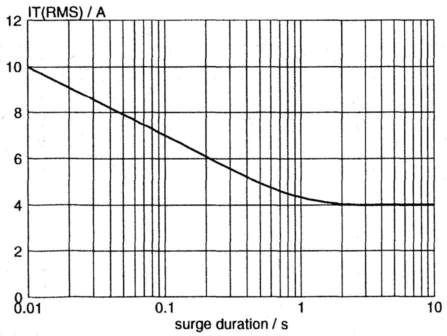


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 92^{\circ}C$.

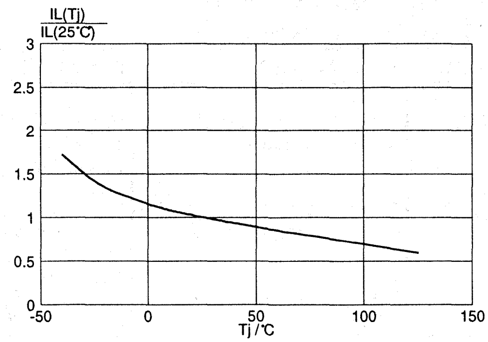


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25^{\circ}C)$, versus junction temperature T_j.

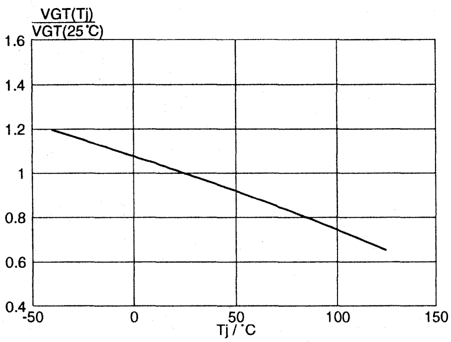


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25^{\circ}C)$, versus junction temperature T_j.

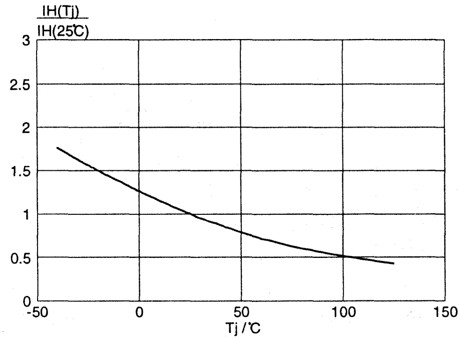


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25^{\circ}C)$, versus junction temperature T_j.

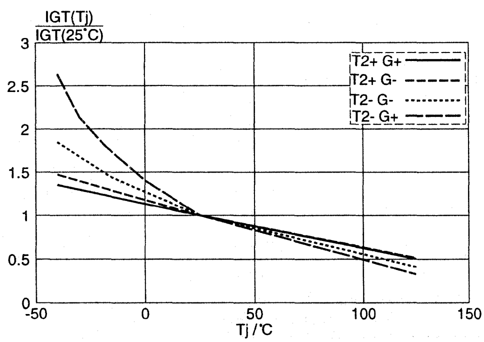


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25^{\circ}C)$, versus junction temperature T_j.

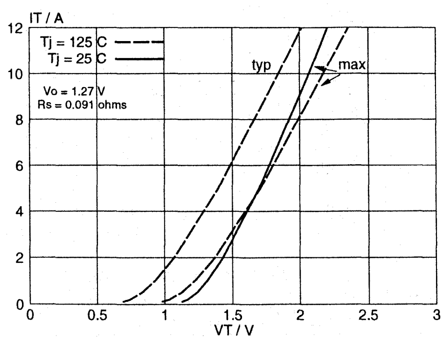


Fig.10. Typical and maximum on-state characteristic.

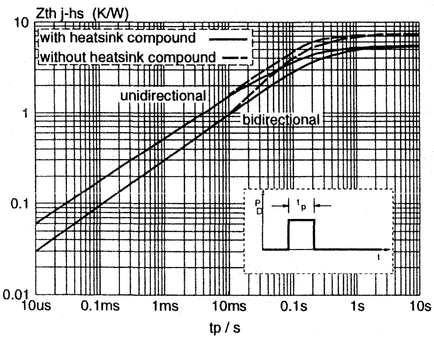


Fig.11. Transient thermal impedance $Z_{th\,j\text{-}hs}$, versus pulse width t_p.

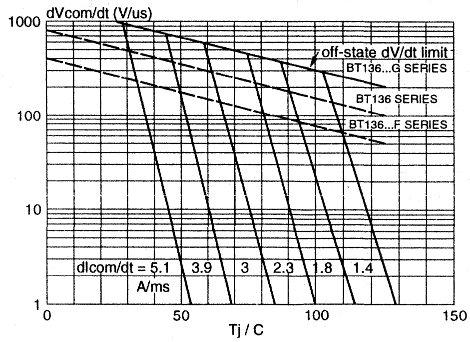


Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation dI_T/dt. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation dI_T/dt.

GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a full pack plastic envelope, intended for use in general purpose bidirectional switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

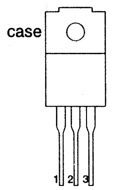
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BT136F-	500D	600D	
V_{DRM}	Repetitive peak off-state voltages	500	600	V
$I_{T(RMS)}$	RMS on-state current	4	4	A
I_{TSM}	Non-repetitive peak on-state current	25	25	A

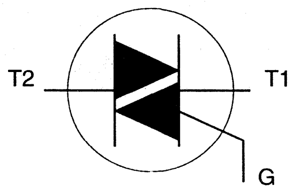
PINNING - SOT186

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
				-500	-600	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{hs} \leq 92$ ˚C	-	4		A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$				
		t = 20 ms	-	25		A
		t = 16.7 ms	-	27		A
I^2t	I^2t for fusing	t = 10 ms	-	3.1		A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 6$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs				
		T2+ G+	-	50		A/µs
		T2+ G-	-	50		A/µs
		T2- G-	-	50		A/µs
		T2- G+	-	10		A/µs
I_{GM}	Peak gate current		-	2		A
V_{GM}	Peak gate voltage		-	5		V
P_{GM}	Peak gate power		-	5		W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5		W
T_{stg}	Storage temperature		-40	150		˚C
T_j	Operating junction temperature		-	125		˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	full or half cycle with heatsink compound without heatsink compound	 - -	 - -	 5.5 7.2	 K/W K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	-	2.0	5	mA
		T2+ G-	-	2.5	5	mA
		T2- G-	-	2.5	5	mA
		T2- G+	-	5.0	10	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	1.6	10	mA
		T2+ G-	-	4.5	15	mA
		T2- G-	-	1.2	10	mA
		T2- G+	-	2.2	15	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	1.2	10	mA
V_T	On-state voltage	I_T = 5 A	-	1.4	1.70	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	$V_D = V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; R_{GK} = 1 kΩ	-	5	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 6 A; $V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs

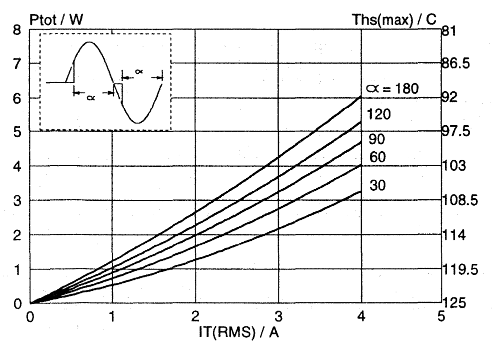


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

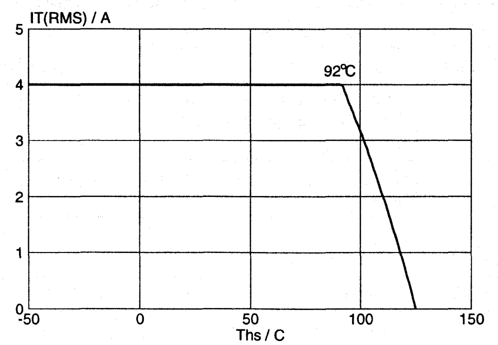


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature T_{hs}.

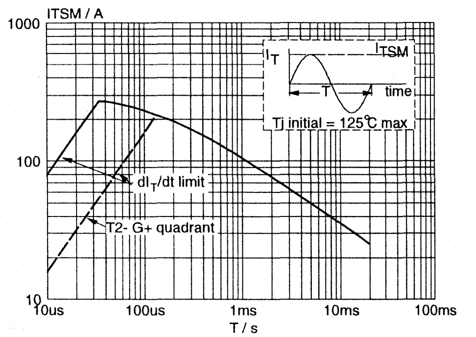


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

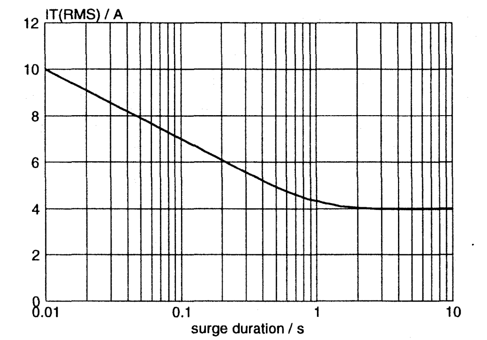


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 92^{\circ}C$.

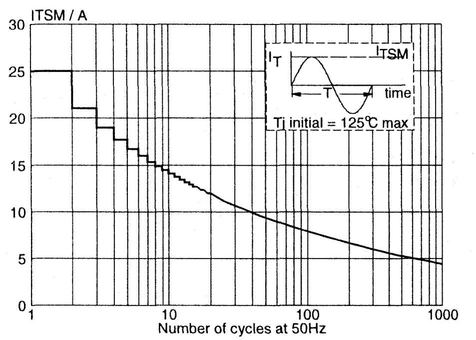


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

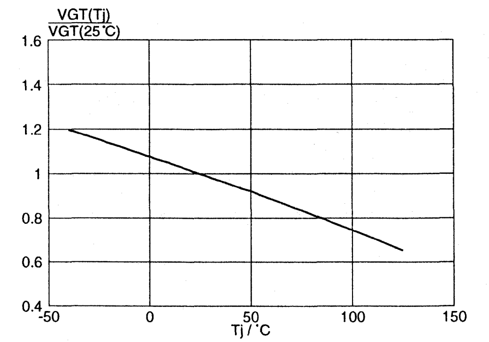


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25^{\circ}C)$, versus junction temperature T_j.

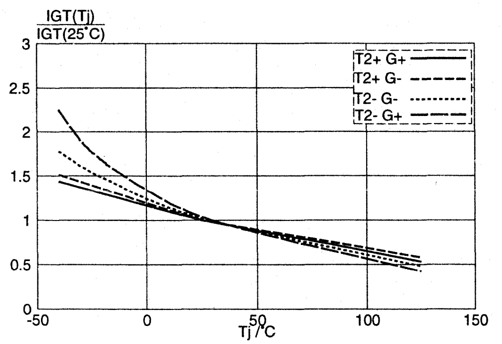


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

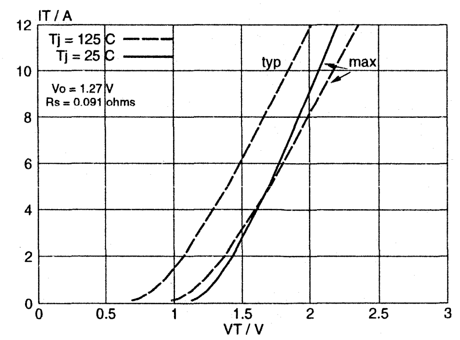


Fig.10. Typical and maximum on-state characteristic.

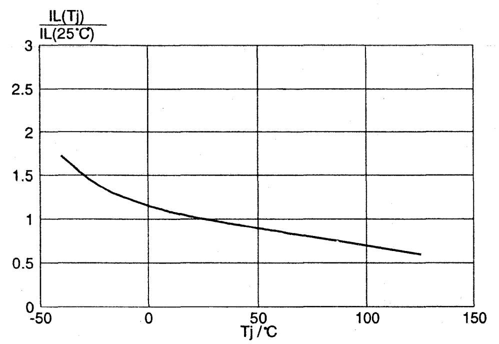


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.

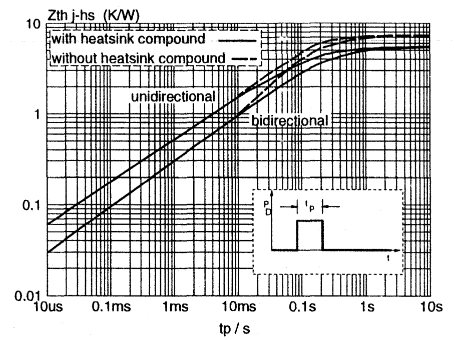


Fig.11. Transient thermal impedance $Z_{th\,j\text{-}hs}$, versus pulse width t_p.

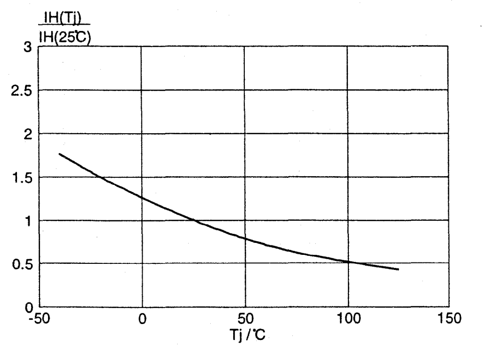


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j.

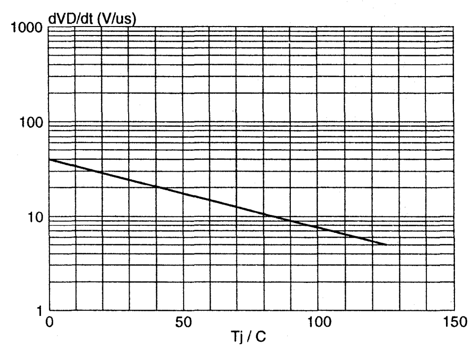


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

Triacs sensitive gate

BT136F series E

GENERAL DESCRIPTION

Glass passivated sensitive gate triacs in a full pack, plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

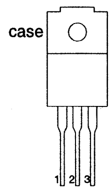
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT136F-	500E	600E	800E	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	4	4	4	A
I_{TSM}	Non-repetitive peak on-state current	25	25	25	A

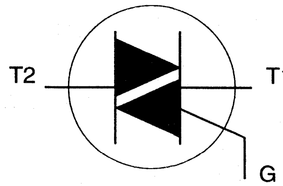
PINNING - SOT186

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	-600	-800	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{hs} \leq 92$ ˚C	-	4			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 20 ms	-	25			A
		t = 16.7 ms	-	27			A
I^2t	I^2t for fusing	t = 10 ms	-	3.1			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 6$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs					
		T2+ G+	-	50			A/µs
		T2+ G-	-	50			A/µs
		T2- G-	-	50			A/µs
		T2- G+	-	10			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	full or half cycle with heatsink compound without heatsink compound	- -	- -	5.5 7.2	K/W K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	-	2.5	10	mA
		T2+ G-	-	4.0	10	mA
		T2- G-	-	5.0	10	mA
		T2- G+	-	11	25	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	3.0	15	mA
		T2+ G-	-	10	20	mA
		T2- G-	-	2.5	15	mA
		T2- G+	-	4.0	20	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	2.2	15	mA
V_T	On-state voltage	I_T = 5 A	-	1.4	1.70	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	-	50	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 6 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs

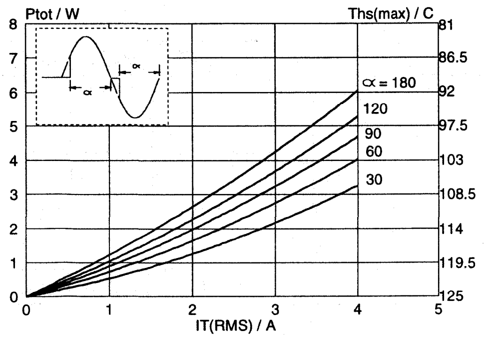


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

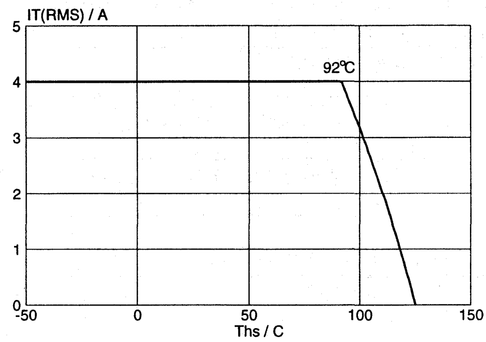


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature T_{hs}.

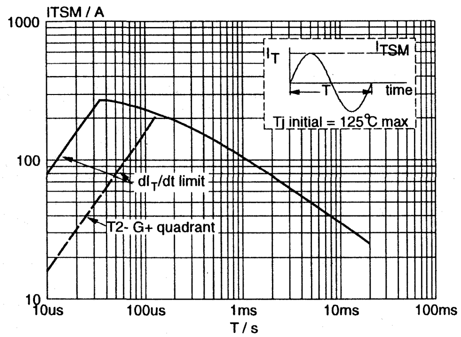


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

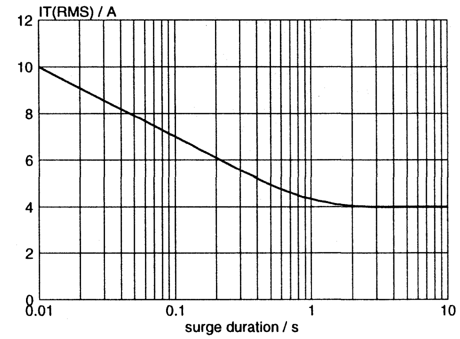


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 92$˚C.

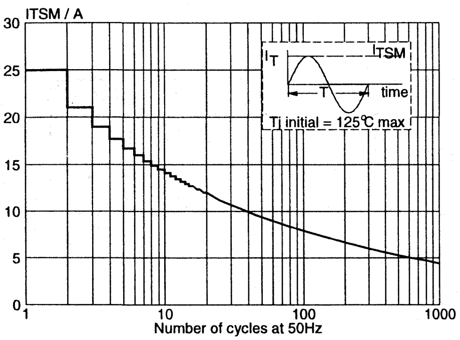


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

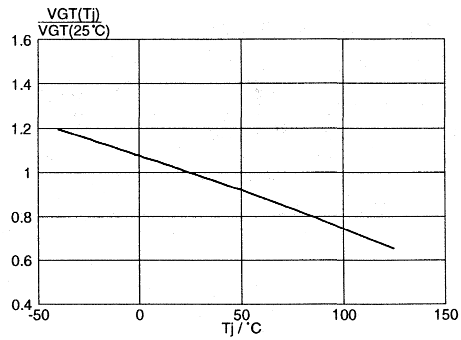


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25˚C)$, versus junction temperature T_j.

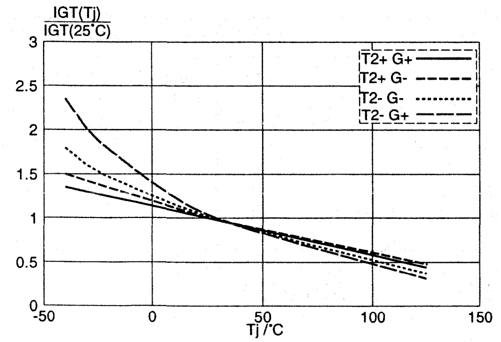


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/I_{GT}(25˚C)$, versus junction temperature T_j.

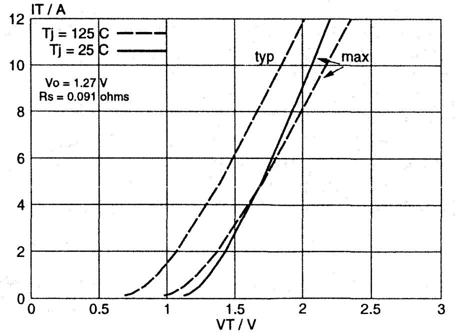


Fig.10. Typical and maximum on-state characteristic.

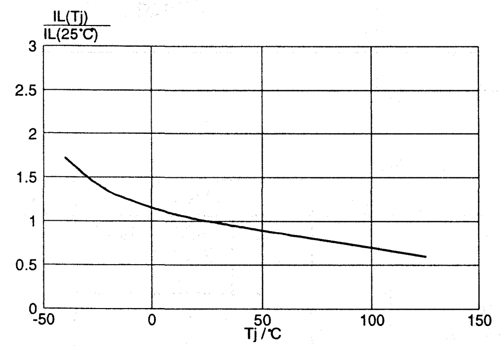


Fig.8. Normalised latching current $I_L(T_j)/I_L(25˚C)$, versus junction temperature T_j.

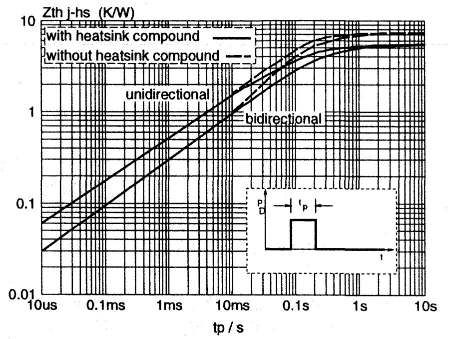


Fig.11. Transient thermal impedance $Z_{th\,j-hs}$, versus pulse width t_p.

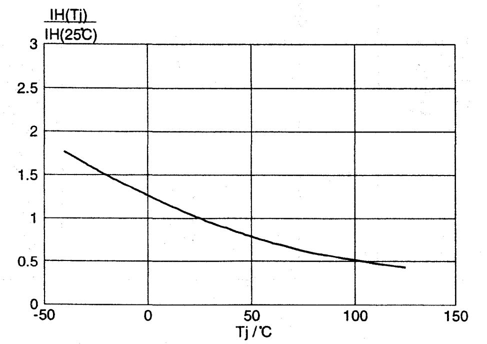


Fig.9. Normalised holding current $I_H(T_j)/I_H(25˚C)$, versus junction temperature T_j.

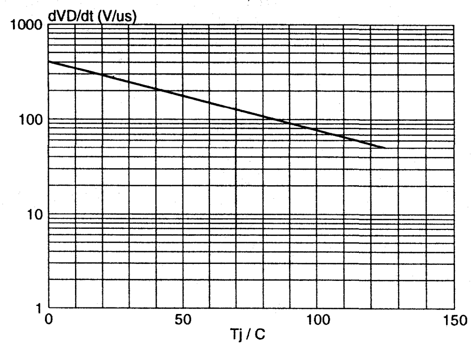


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

GENERAL DESCRIPTION

Glass passivated triacs in a full pack plastic envelope, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

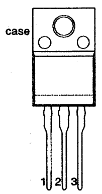
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT136X-	**500**	**600**	**800**	
	BT136X-	**500F**	**600F**	**800F**	
	BT136X-	**500G**	**600G**	**800G**	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	4	4	4	A
I_{TSM}	Non-repetitive peak on-state current	25	25	25	A

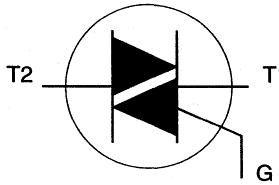
PINNING - SOT186A

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	**-600**	**-800**	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{hs} \leq 92$ ˚C	-	4			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 20 ms	-	25			A
		t = 16.7 ms	-	27			A
I^2t	I^2t for fusing	t = 10 ms	-	3.1			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 6$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs					
		T2+ G+	-	50			A/µs
		T2+ G-	-	50			A/µs
		T2- G-	-	50			A/µs
		T2- G+	-	10			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-hs}$	Thermal resistance junction to heatsink	full or half cycle				
		with heatsink compound	-	-	5.5	K/W
		without heatsink compound	-	-	7.2	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	in free air	-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.			UNIT
		BT136X-			...	...F	...G	
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A						
		T2+ G+	-	5	35	25	50	mA
		T2+ G-	-	8	35	25	50	mA
		T2- G-	-	11	35	25	50	mA
		T2- G+	-	30	70	70	100	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A						
		T2+ G+	-	7	20	20	30	mA
		T2+ G-	-	16	30	30	45	mA
		T2- G-	-	5	20	20	30	mA
		T2- G+	-	7	30	30	45	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	5	15	15	30	mA
V_T	On-state voltage	I_T = 5 A	-	1.4	1.70			V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5			V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-			V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5			mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.			TYP.	MAX.	UNIT
		BT136X-	**...**	**...F**	**...G**			
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	100	50	200	250	-	V/μs
dV_{com}/dt	Critical rate of change of commutating voltage	V_{DM} = 400 V; T_j = 95 ˚C; $I_{T(RMS)}$ = 4 A; dI_{com}/dt = 1.8 A/ms; gate open circuit	-	-	10	50	-	V/μs
t_{gt}	Gate controlled turn-on time	I_{TM} = 6 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/μs	-	-	-	2	-	μs

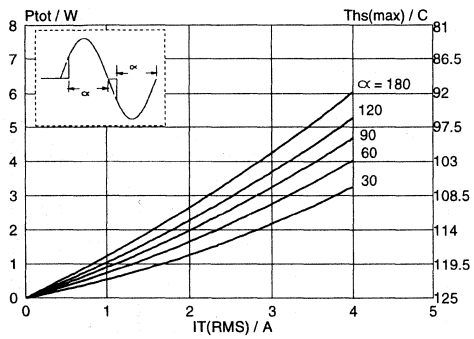


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

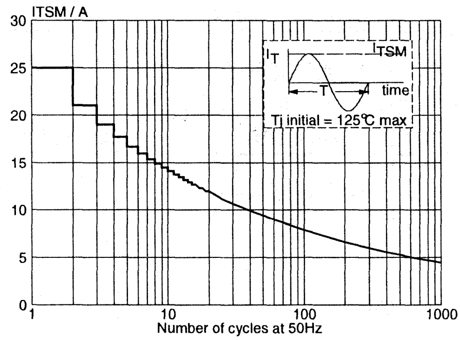


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

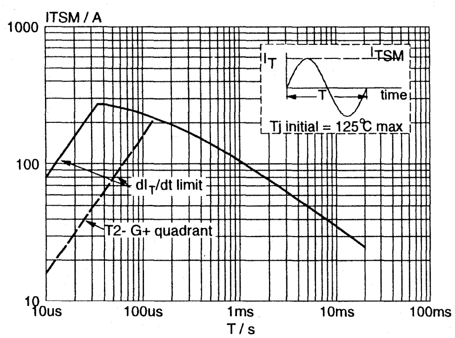


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq$ 20ms.

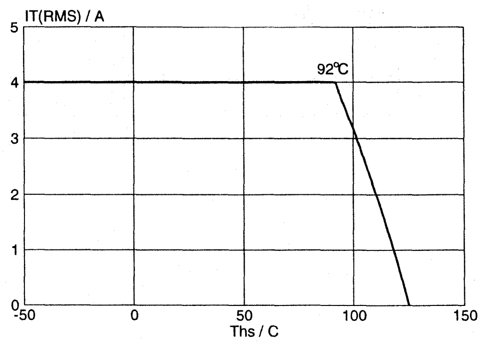


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature T_{hs}.

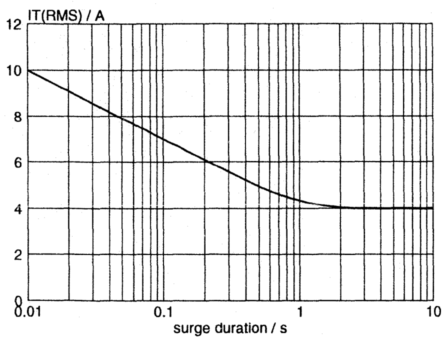


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 92˚C$.

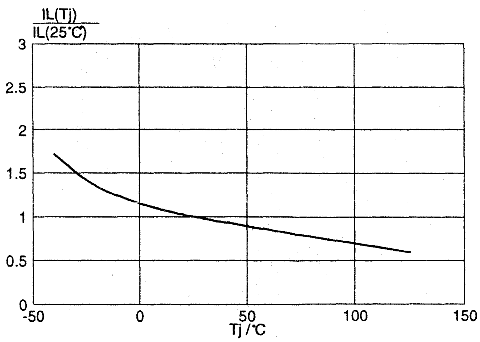


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.

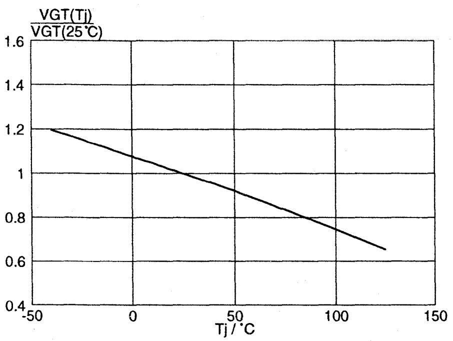


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25˚C)$, versus junction temperature T_j.

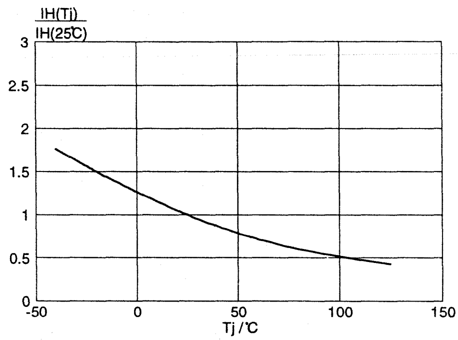


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j.

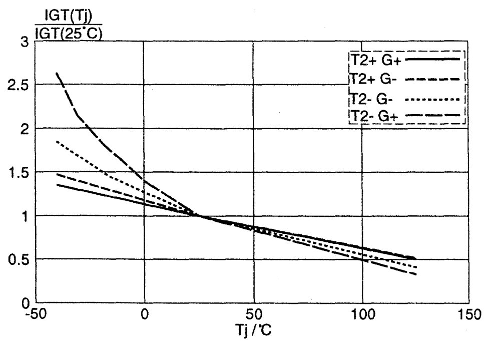


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

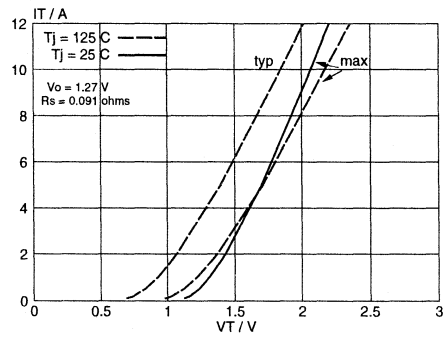


Fig.10. Typical and maximum on-state characteristic.

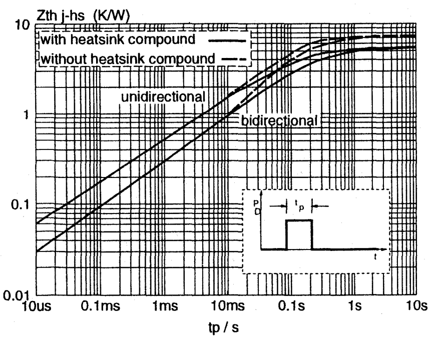


Fig.11. Transient thermal impedance $Z_{th\,j\text{-}hs}$, versus pulse width t_p.

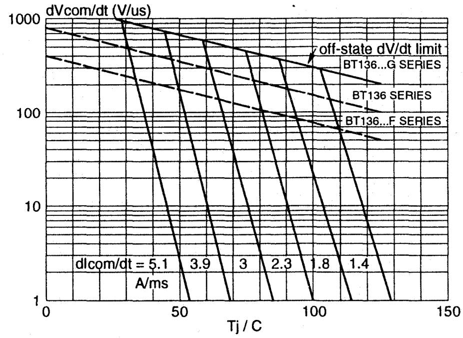


Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation dI_T/dt. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation dI_T/dt.

GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a full pack plastic envelope, intended for use in general purpose bidirectional switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

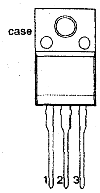
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BT136X-	500D	600D	
V_{DRM}	Repetitive peak off-state voltages	500	600	V
$I_{T(RMS)}$	RMS on-state current	4	4	A
I_{TSM}	Non-repetitive peak on-state current	25	25	A

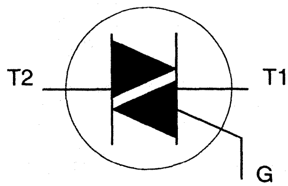
PINNING - SOT186A

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
				-500	-600	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{hs} \leq 92$ ˚C	-	4		A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$				
		t = 20 ms	-	25		A
		t = 16.7 ms	-	27		A
I^2t	I^2t for fusing	t = 10 ms	-	3.1		A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 6$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs				
		T2+ G+	-	50		A/µs
		T2+ G-	-	50		A/µs
		T2- G-	-	50		A/µs
		T2- G+	-	10		A/µs
I_{GM}	Peak gate current		-	2		A
V_{GM}	Peak gate voltage		-	5		V
P_{GM}	Peak gate power		-	5		W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5		W
T_{stg}	Storage temperature		-40	150		˚C
T_j	Operating junction temperature		-	125		˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-hs}$	Thermal resistance junction to heatsink	full or half cycle				
		with heatsink compound	-	-	5.5	K/W
		without heatsink compound	-	-	7.2	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	in free air	-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	-	2.0	5	mA
		T2+ G-	-	2.5	5	mA
		T2- G-	-	2.5	5	mA
		T2- G+	-	5.0	10	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	1.6	10	mA
		T2+ G-	-	4.5	15	mA
		T2- G-	-	1.2	10	mA
		T2- G+	-	2.2	15	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	1.2	10	mA
V_T	On-state voltage	I_T = 5 A	-	1.4	1.70	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; R_{GK} = 1 kΩ	-	5	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 6 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs

Triacs logic level

BT136X series D

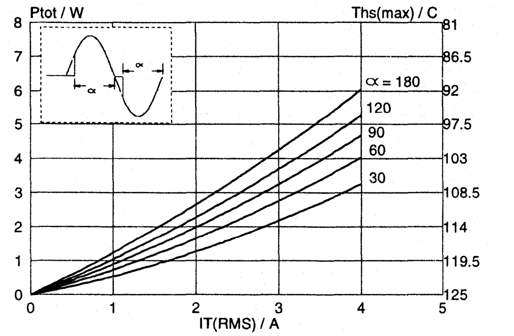


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

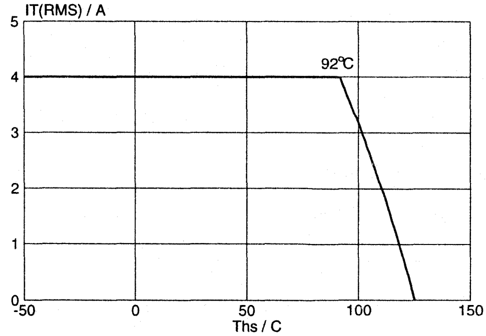


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature T_{hs}.

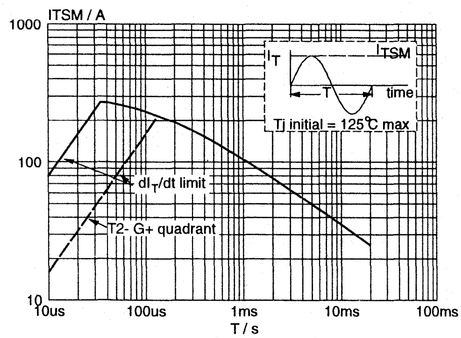


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

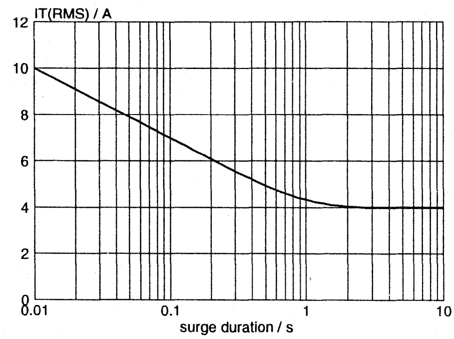


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 92^{\circ}C$.

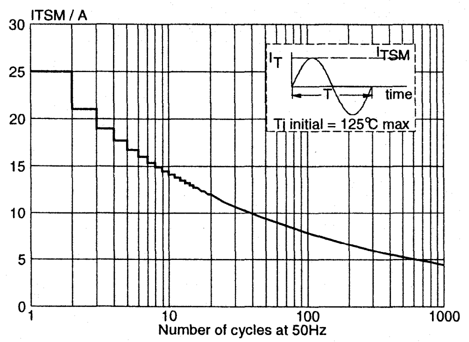


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

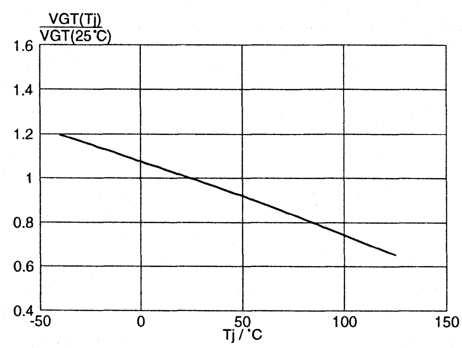


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25^{\circ}C)$, versus junction temperature T_j.

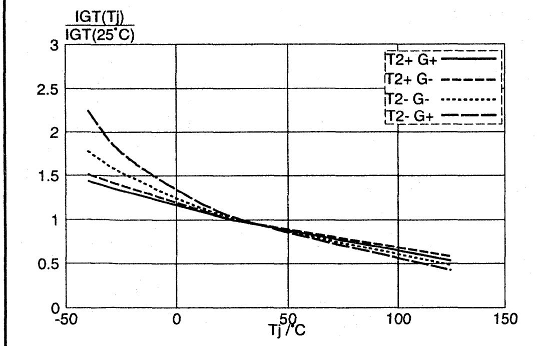


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/I_{GT}(25˚C)$, versus junction temperature T_j.

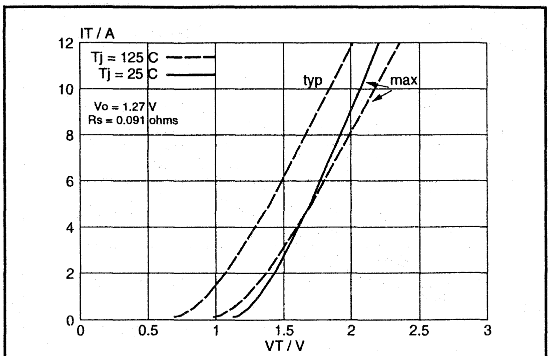


Fig.10. Typical and maximum on-state characteristic.

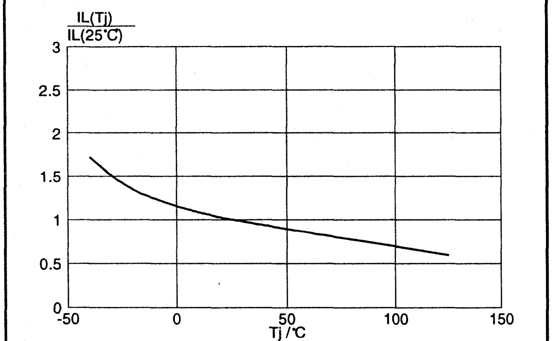


Fig.8. Normalised latching current $I_L(T_j)/I_L(25˚C)$, versus junction temperature T_j.

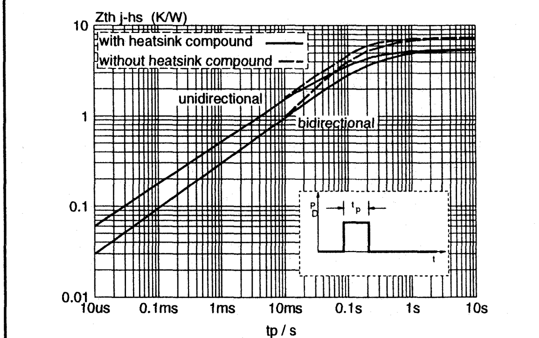


Fig.11. Transient thermal impedance $Z_{th\,j\text{-}hs}$, versus pulse width t_p.

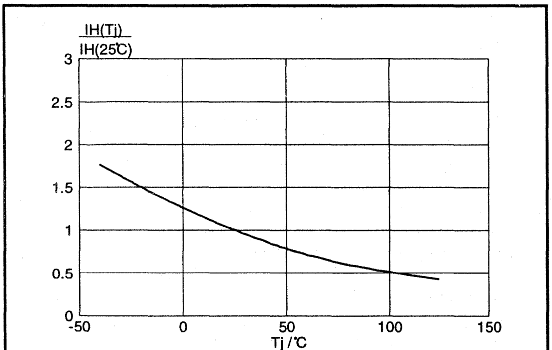


Fig.9. Normalised holding current $I_H(T_j)/I_H(25˚C)$, versus junction temperature T_j.

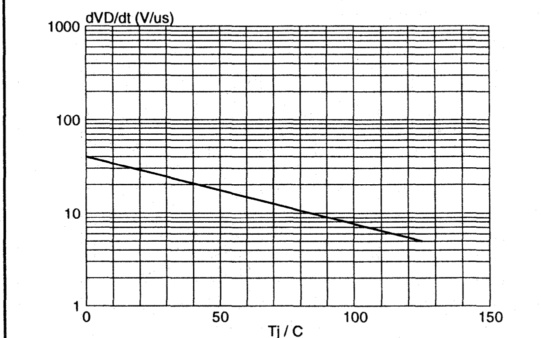


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a full pack plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

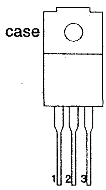
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT136X-	500E	600E	800E	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	4	4	4	A
I_{TSM}	Non-repetitive peak on-state current	25	25	25	A

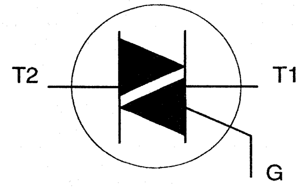
PINNING - SOT186

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	-600	-800	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{hs} \leq 92$ ˚C	-	4			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 20 ms	-	25			A
		t = 16.7 ms	-	27			A
I^2t	I^2t for fusing	t = 10 ms	-	3.1			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 6$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs					
		T2+ G+	-	50			A/µs
		T2+ G-	-	50			A/µs
		T2- G-	-	50			A/µs
		T2- G+	-	10			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	full or half cycle with heatsink compound	-	-	5.5	K/W
		without heatsink compound	-	-	7.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	-	2.5	10	mA
		T2+ G-	-	4.0	10	mA
		T2- G-	-	5.0	10	mA
		T2- G+	-	11	25	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	3.0	15	mA
		T2+ G-	-	10	20	mA
		T2- G-	-	2.5	15	mA
		T2- G+	-	4.0	20	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	2.2	15	mA
V_T	On-state voltage	I_T = 5 A	-	1.4	1.70	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	-	50	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 6 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs

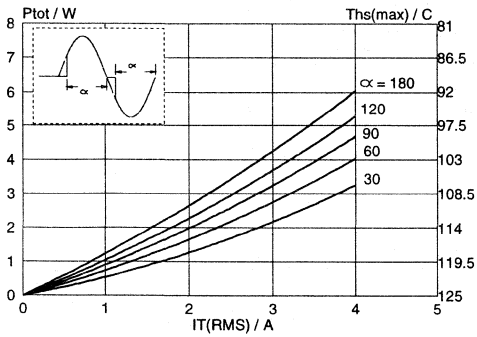


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

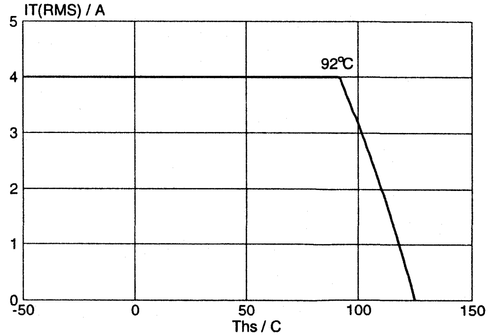


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature T_{hs}.

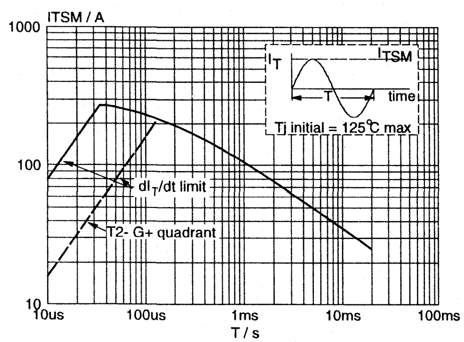


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

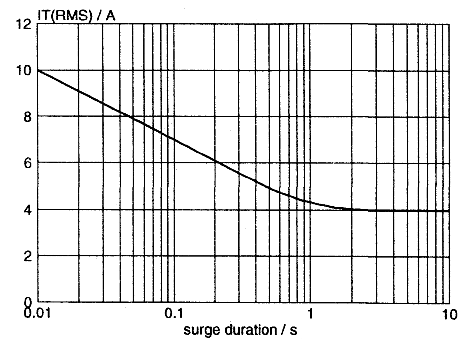


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 92°C$.

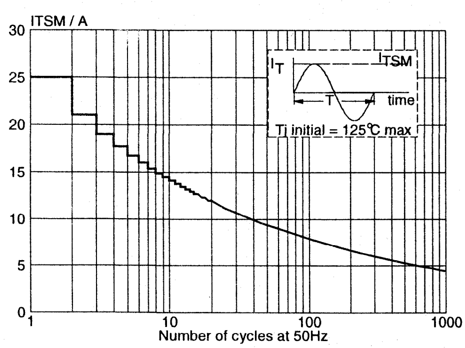


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

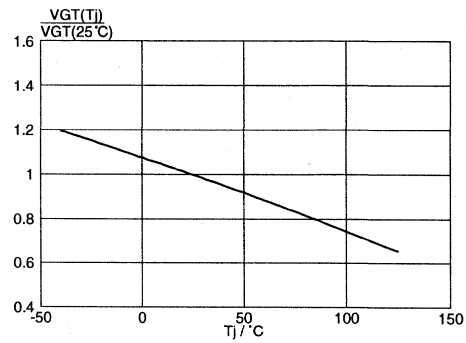


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25°C)$, versus junction temperature T_j.

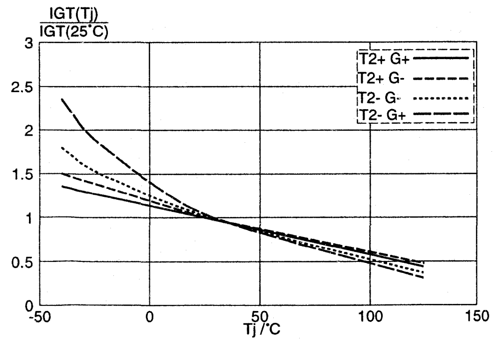


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

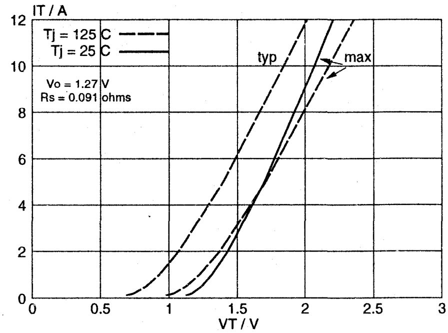


Fig.10. Typical and maximum on-state characteristic.

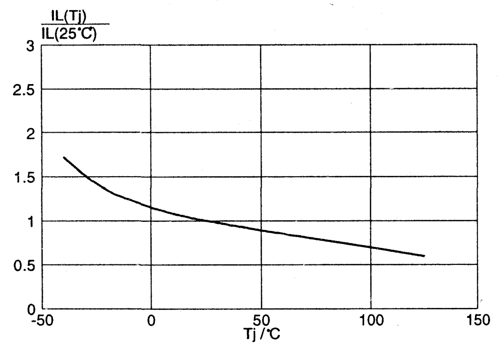


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.

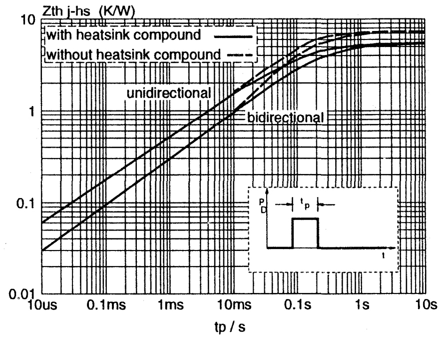


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}hs}$, versus pulse width t_p.

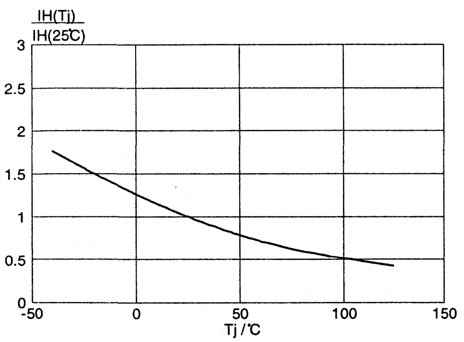


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j.

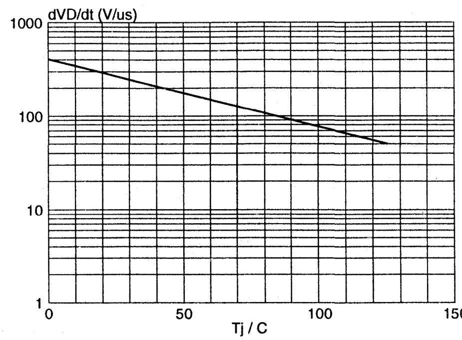


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

GENERAL DESCRIPTION

Glass passivated triacs in a plastic envelope, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

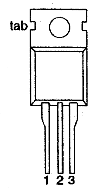
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT137-	**500**	**600**	**800**	
	BT137-	**500F**	**600F**	**800F**	
	BT137-	**500G**	**600G**	**800G**	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	8	8	8	A
I_{TSM}	Non-repetitive peak on-state current	55	55	55	A

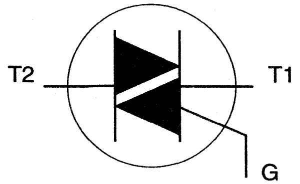
PINNING - TO220AB

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
tab	main terminal 2

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	**-600**	**-800**	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 102$ °C	-	8			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ °C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 20 ms	-	55			A
		t = 16.7 ms	-	60			A
I^2t	I^2t for fusing	t = 10 ms	-	15			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 12$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs					
		T2+ G+	-	50			A/µs
		T2+ G-	-	50			A/µs
		T2- G-	-	50			A/µs
		T2- G+	-	10			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			°C
T_j	Operating junction temperature		-	125			°C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\,j\text{-}mb}$	Thermal resistance junction to mounting base	full cycle	-	-	2.0	K/W
		half cycle	-	-	2.4	K/W
$R_{th\,j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.			UNIT
		BT137-			...	...F	...G	
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A						
		T2+ G+	-	5	35	25	50	mA
		T2+ G-	-	8	35	25	50	mA
		T2- G-	-	11	35	25	50	mA
		T2- G+	-	30	70	70	100	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A						
		T2+ G+	-	7	30	30	45	mA
		T2+ G-	-	16	45	45	60	mA
		T2- G-	-	5	30	30	45	mA
		T2- G+	-	7	45	45	60	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	5	20	20	40	mA
V_T	On-state voltage	I_T = 10 A	-	1.3	1.65			V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5			V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-			V
I_D	Off-state leakage current	$V_D = V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5			mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.			TYP.	MAX.	UNIT
		BT137-	...	...F	...G			
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	100	50	200	250	-	V/µs
dV_{com}/dt	Critical rate of change of commutating voltage	V_{DM} = 400 V; T_j = 95 ˚C; $I_{T(RMS)}$ = 8 A; dI_{com}/dt = 3.6 A/ms; gate open circuit	-	-	10	20	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 12 A; $V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	-	-	2	-	µs

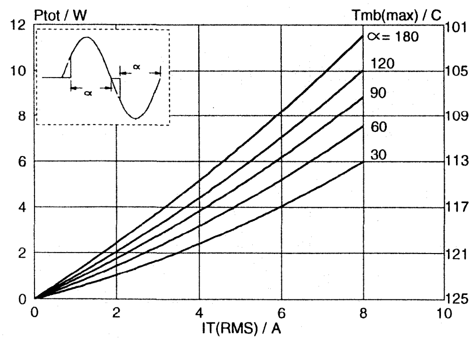


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

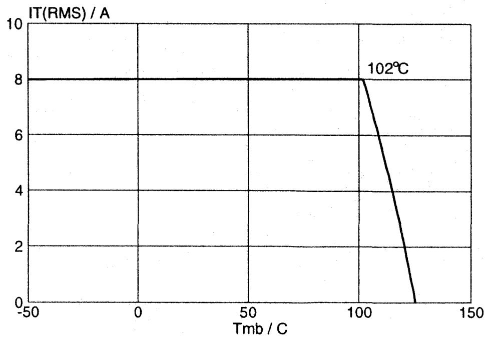


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

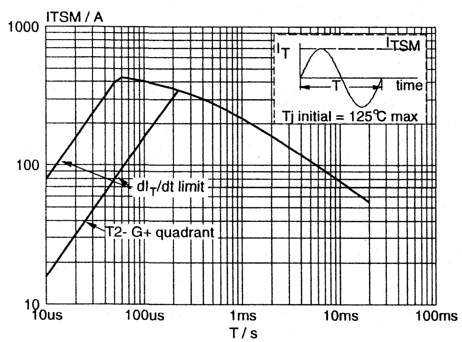


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq$ 20ms.

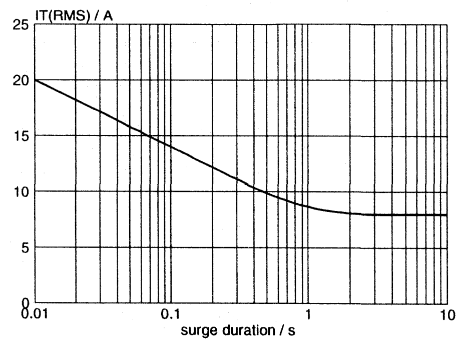


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq$ 102˚C.

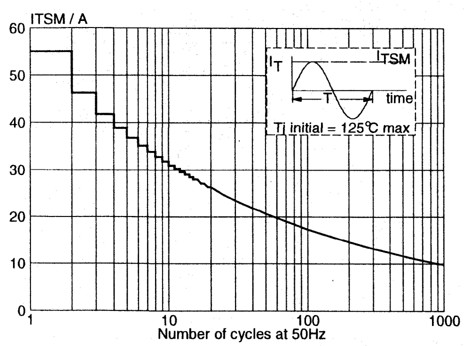


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

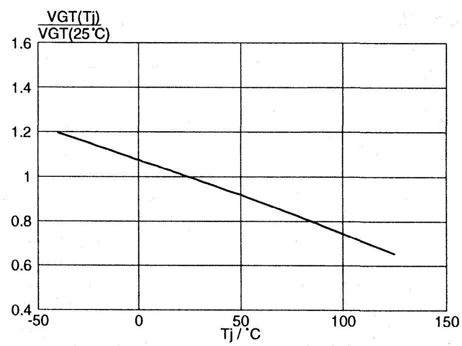


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)$/ V_{GT}(25˚C), versus junction temperature T_j.

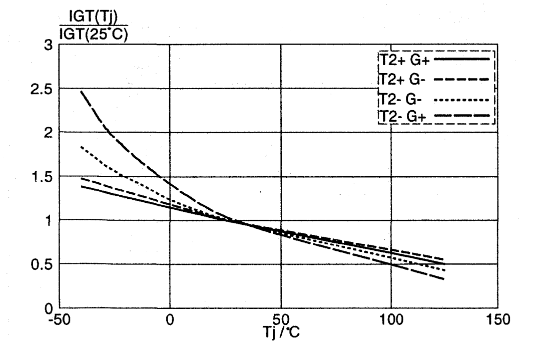


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

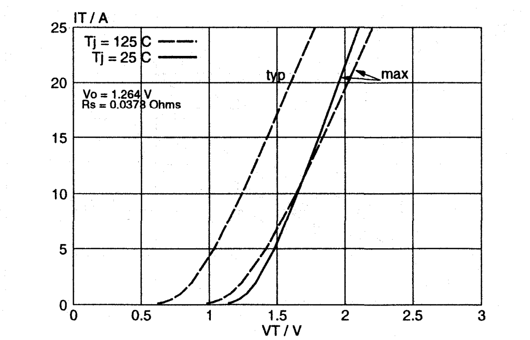


Fig.10. Typical and maximum on-state characteristic.

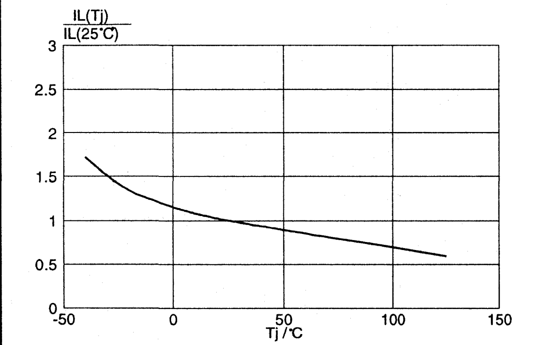


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.

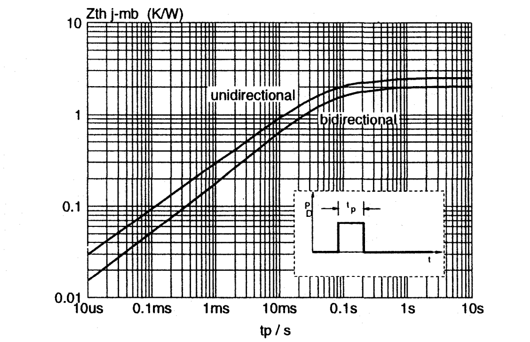


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width t_p.

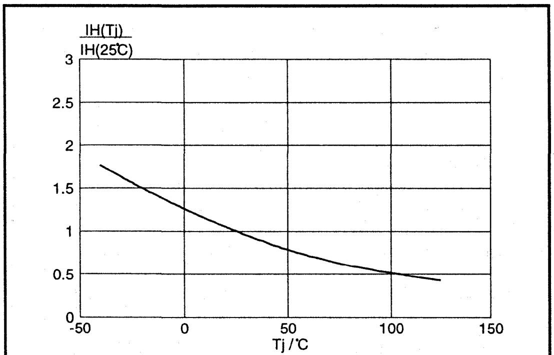


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j.

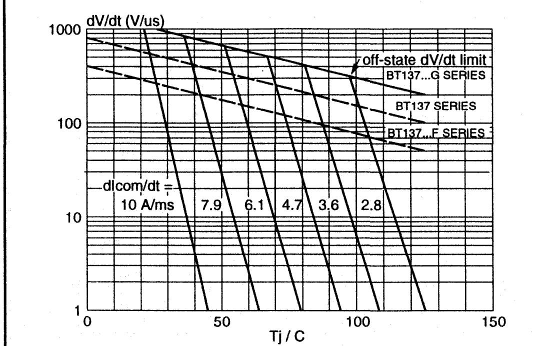


Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation dI_T/dt. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation dI_T/dt.

GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

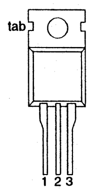
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BT137-	**500D**	**600D**	
V_{DRM}	Repetitive peak off-state voltages	500	600	V
$I_{T(RMS)}$	RMS on-state current	8	8	A
I_{TSM}	Non-repetitive peak on-state current	55	55	A

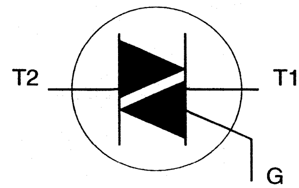
PINNING - TO220AB

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
tab	main terminal 2

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
				-500	**-600**	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 102$ ˚C	-	8		A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$				
		t = 20 ms	-	55		A
		t = 16.7 ms	-	60		A
I^2t	I^2t for fusing	t = 10 ms	-	15		A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 12$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs				
		T2+ G+	-	50		A/µs
		T2+ G-	-	50		A/µs
		T2- G-	-	50		A/µs
		T2- G+	-	10		A/µs
I_{GM}	Peak gate current		-	2		A
V_{GM}	Peak gate voltage		-	5		V
P_{GM}	Peak gate power		-	5		W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5		W
T_{stg}	Storage temperature		-40	150		˚C
T_j	Operating junction temperature		-	125		˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	full cycle	-	-	2.0	K/W
		half cycle	-	-	2.4	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	-	2.5	5	mA
		T2+ G-	-	3.5	5	mA
		T2- G-	-	3.5	5	mA
		T2- G+	-	6.5	10	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	1.6	15	mA
		T2+ G-	-	8.5	20	mA
		T2- G-	-	1.2	15	mA
		T2- G+	-	2.5	20	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	1.5	10	mA
V_T	On-state voltage	I_T = 10 A	-	1.3	1.65	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; R_{GK} = 1 kΩ	-	5	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 12 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs

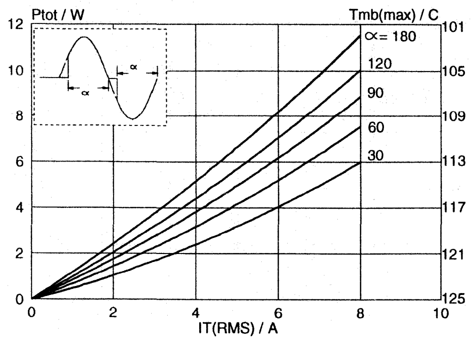


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

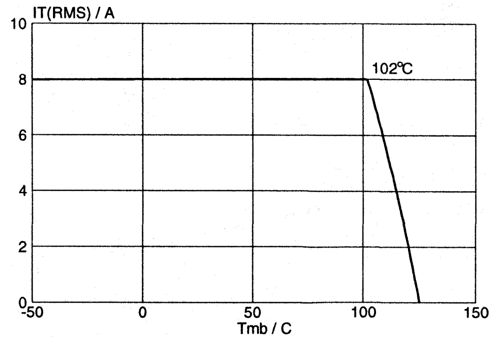


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

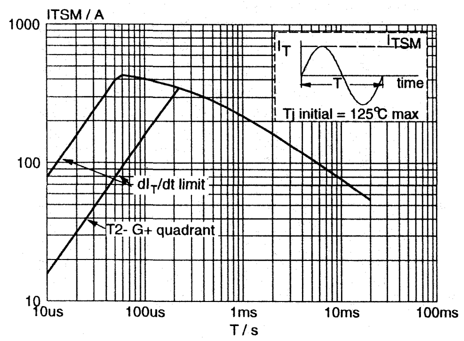


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

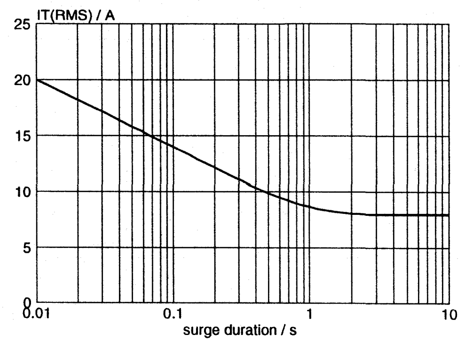


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 102$˚C.

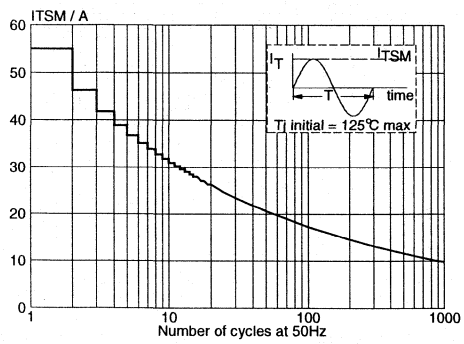


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

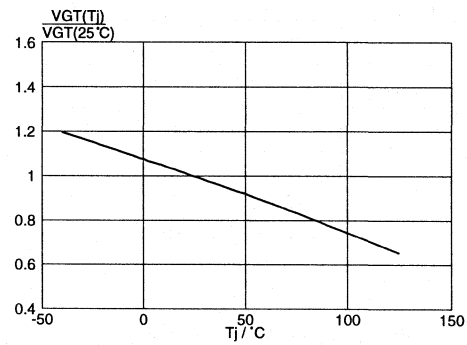


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)$/ V_{GT}(25˚C), versus junction temperature T_j.

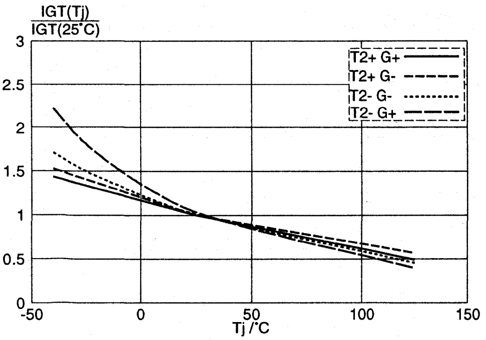


Fig.7. *Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.*

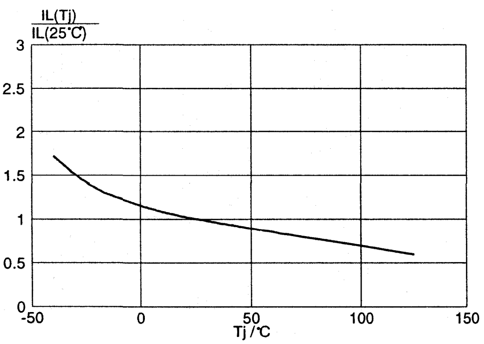


Fig.8. *Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.*

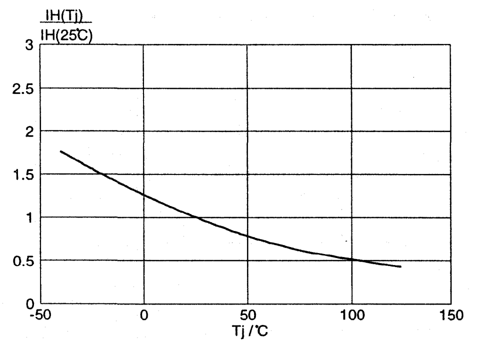


Fig.9. *Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j.*

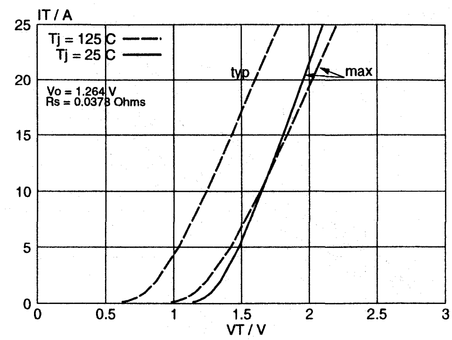


Fig.10. *Typical and maximum on-state characteristic.*

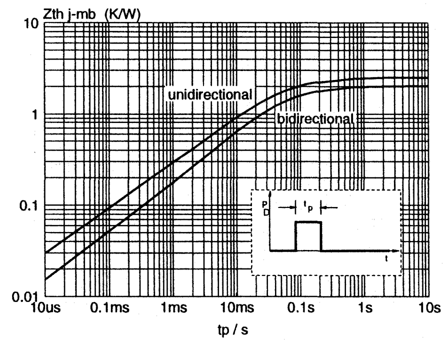


Fig.11. *Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width t_p.*

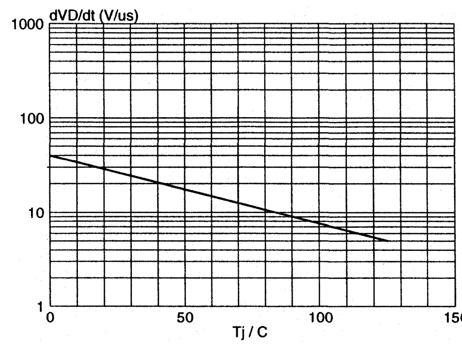


Fig.12. *Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.*

Triacs sensitive gate

BT137 series E

GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

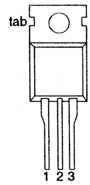
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT137-	500E	600E	800E	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	8	8	8	A
I_{TSM}	Non-repetitive peak on-state current	55	55	55	A

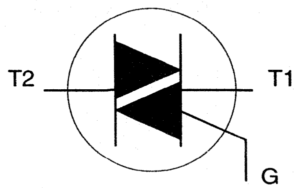
PINNING - TO220AB

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
tab	main terminal 2

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	-600	-800	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 102$ ˚C	-	8			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 20 ms	-	55			A
		t = 16.7 ms	-	60			A
I^2t	I^2t for fusing	t = 10 ms	-	15			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	I_{TM} = 12 A; I_G = 0.2 A; dI_G/dt = 0.2 A/µs					
		T2+ G+	-	50			A/µs
		T2+ G-	-	50			A/µs
		T2- G-	-	50			A/µs
		T2- G+	-	10			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	full cycle	-	-	2.0	K/W
		half cycle	-	-	2.4	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	-	2.5	10	mA
		T2+ G-	-	4.0	10	mA
		T2- G-	-	5.0	10	mA
		T2- G+	-	11	25	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	3.0	25	mA
		T2+ G-	-	14	35	mA
		T2- G-	-	3.0	25	mA
		T2- G+	-	4.0	35	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	2.5	20	mA
V_T	On-state voltage	I_T = 10 A	-	1.3	1.65	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	$V_D = V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	-	50	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 12 A; $V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs

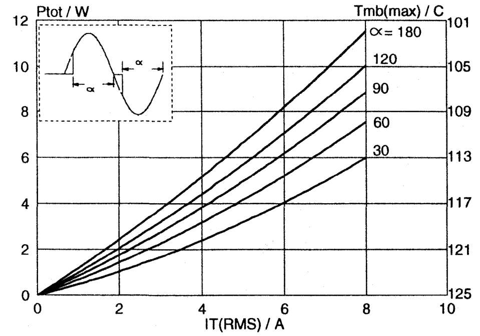


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

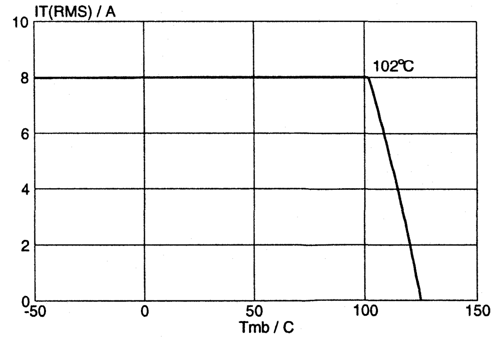


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

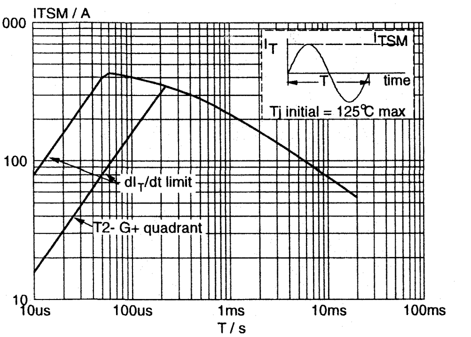


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20$ms.

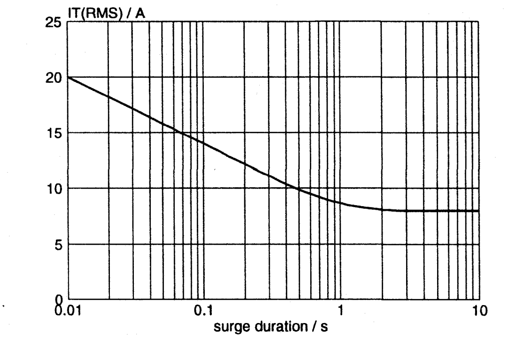


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 102$˚C.

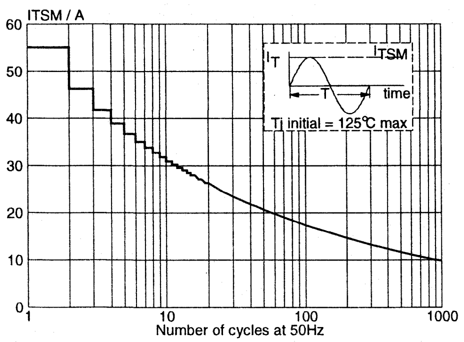


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

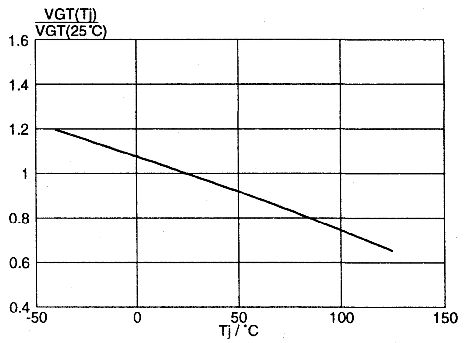


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25˚C)$, versus junction temperature T_j.

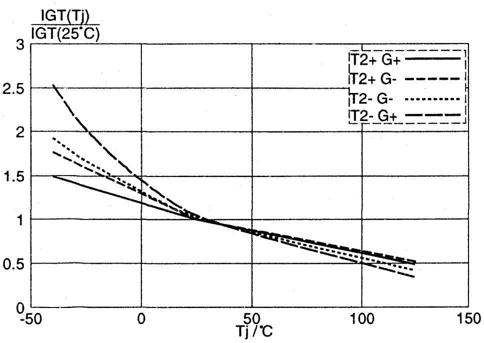


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

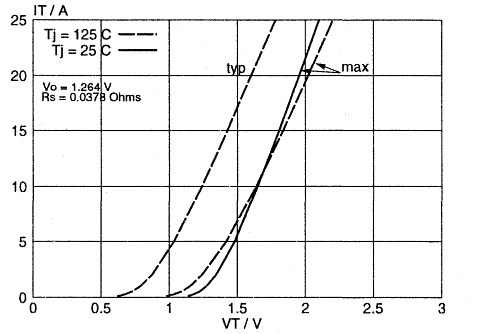


Fig.10. Typical and maximum on-state characteristic.

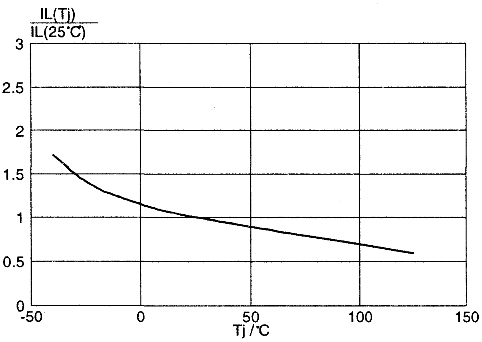


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.

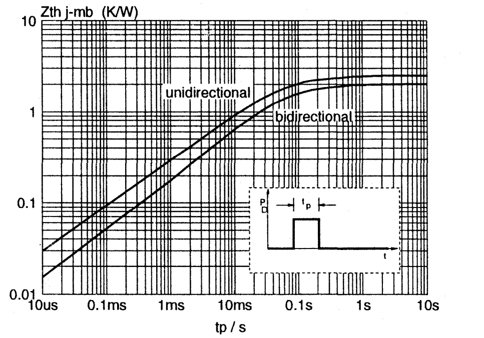


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width t_p.

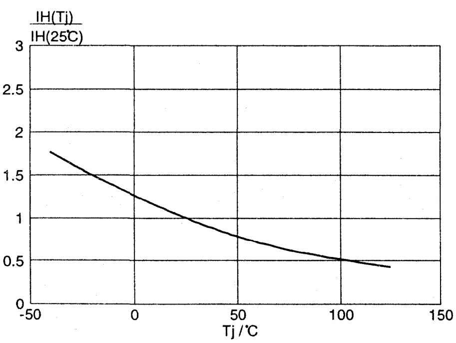


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j.

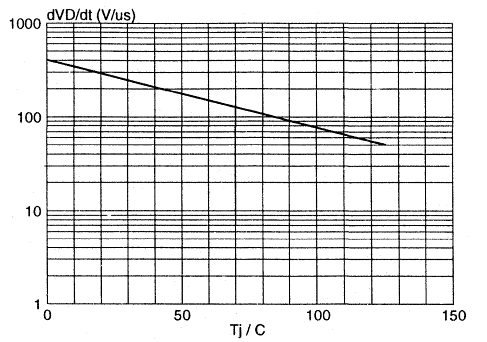


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

GENERAL DESCRIPTION

Glass passivated triacs in a full pack plastic envelope, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

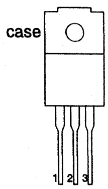
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT137F-	**500**	**600**	**800**	
	BT137F-	**500F**	**600F**	**800F**	
	BT137F-	**500G**	**600G**	**800G**	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	8	8	8	A
I_{TSM}	Non-repetitive peak on-state current	55	55	55	A

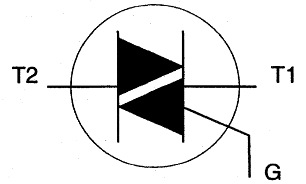
PINNING - SOT186

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	**-600**	**-800**	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{hs} \leq 73$ ˚C	-	8			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 20 ms	-	55			A
		t = 16.7 ms	-	60			A
I^2t	I^2t for fusing	t = 10 ms	-	15			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 12$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs					
		T2+ G+	-	50			A/µs
		T2+ G-	-	50			A/µs
		T2- G-	-	50			A/µs
		T2- G+	-	10			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	full or half cycle with heatsink compound	-	-	4.5	K/W
		without heatsink compound	-	-	6.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.			UNIT
		BT137F-			...	...F	...G	
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A						
		T2+ G+	-	5	35	25	50	mA
		T2+ G-	-	8	35	25	50	mA
		T2- G-	-	11	35	25	50	mA
		T2- G+	-	30	70	70	100	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A						
		T2+ G+	-	7	30	30	45	mA
		T2+ G-	-	16	45	45	60	mA
		T2- G-	-	5	30	30	45	mA
		T2- G+	-	7	45	45	60	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	5	20	20	40	mA
V_T	On-state voltage	I_T = 10 A	-	1.3	1.65			V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5			V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-			V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5			mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.			TYP.	MAX.	UNIT
		BT137F-	...	...F	...G			
dV_D/dt	Critical rate of change of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	100	50	200	250	-	V/μs
dV_{com}/dt	Critical rate of change of commutating voltage	V_{DM} = 400 V; T_j = 95 ˚C; $I_{T(RMS)}$ = 8 A; dI_{com}/dt = 3.6 A/ms; gate open circuit	-	-	10	20	-	V/μs
t_{gt}	Gate controlled turn-on time	I_{TM} = 12 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/μs	-	-	-	2	-	μs

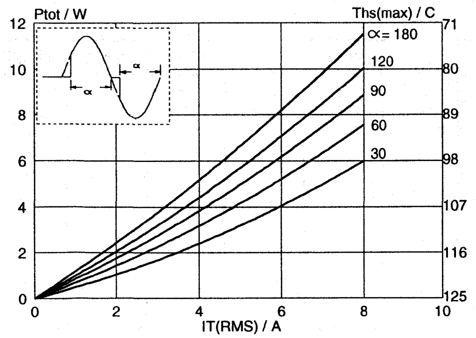


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

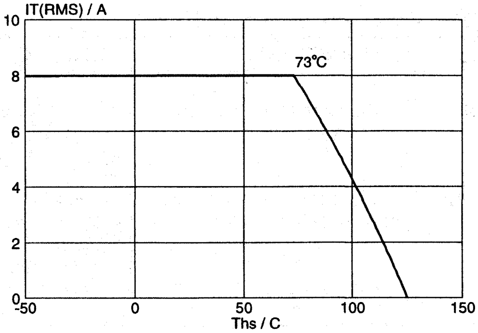


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature T_{hs}.

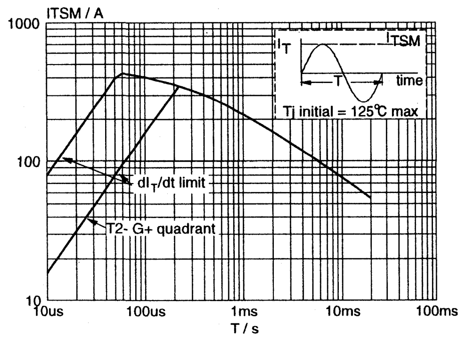


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

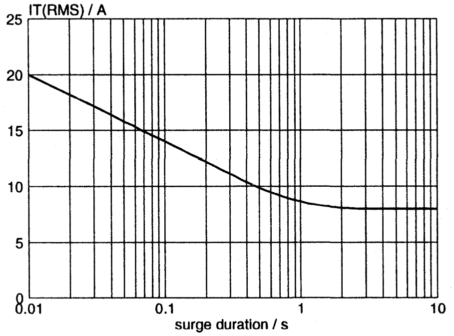


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 73^{\circ}C$.

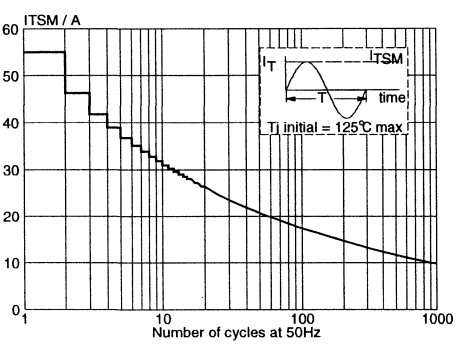


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

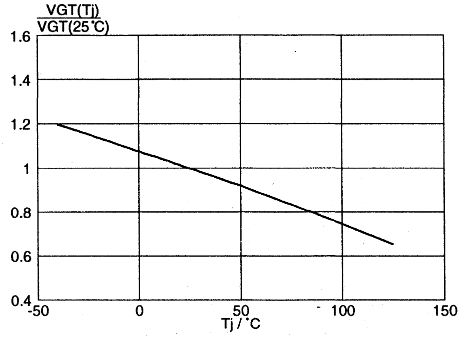


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25^{\circ}C)$, versus junction temperature T_j.

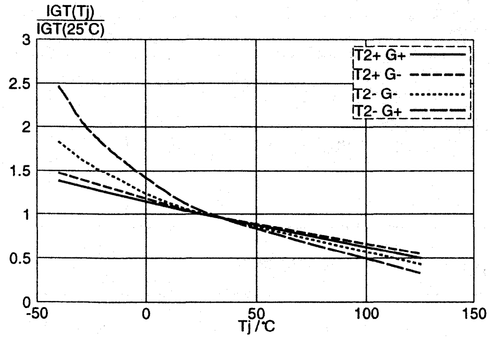


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/I_{GT}(25˚C)$, versus junction temperature T_j.

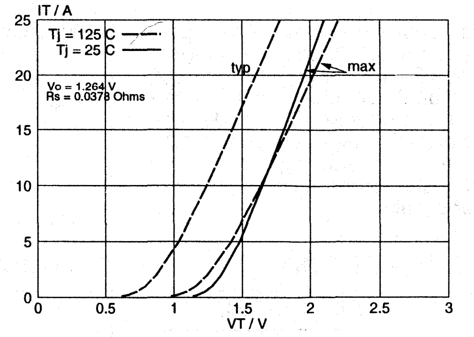


Fig.10. Typical and maximum on-state characteristic.

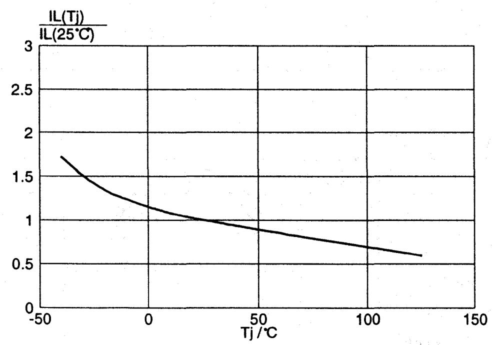


Fig.8. Normalised latching current $I_L(T_j)/I_L(25˚C)$, versus junction temperature T_j.

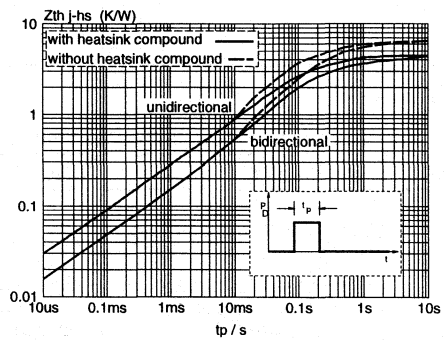


Fig.11. Transient thermal impedance $Z_{th\,j\text{-}hs}$, versus pulse width t_p.

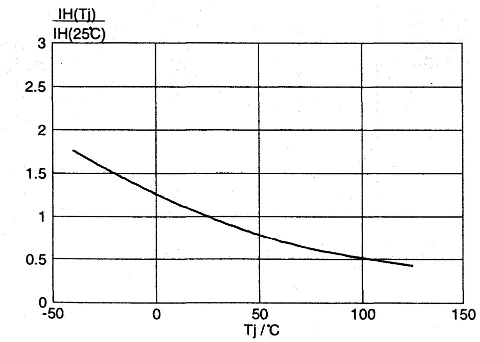


Fig.9. Normalised holding current $I_H(T_j)/I_H(25˚C)$, versus junction temperature T_j.

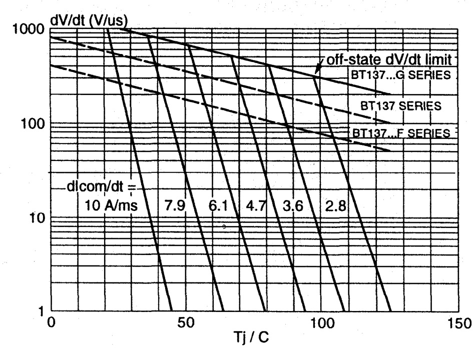


Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation dI_T/dt. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation dI_T/dt.

Triacs logic level

BT137F series D

GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a full pack plastic envelope, intended for use in general purpose bidirectional switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

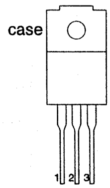
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BT137F-	**500D**	**600D**	
V_{DRM}	Repetitive peak off-state voltages	500	600	V
$I_{T(RMS)}$	RMS on-state current	8	8	A
I_{TSM}	Non-repetitive peak on-state current	55	55	A

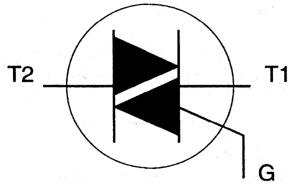
PINNING - SOT186

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
				-500	**-600**	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{hs} \leq 73$ ˚C	-	8		A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$				
		t = 20 ms	-	55		A
		t = 16.7 ms	-	60		A
I^2t	I^2t for fusing	t = 10 ms	-	15		A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 12$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs				
		T2+ G+	-	50		A/µs
		T2+ G-	-	50		A/µs
		T2- G-	-	50		A/µs
		T2- G+	-	10		A/µs
I_{GM}	Peak gate current		-	2		A
V_{GM}	Peak gate voltage		-	5		V
P_{GM}	Peak gate power		-	5		W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5		W
T_{stg}	Storage temperature		-40	150		˚C
T_j	Operating junction temperature		-	125		˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-hs}$	Thermal resistance junction to heatsink	full or half cycle				
		with heatsink compound	-	-	4.5	K/W
		without heatsink compound	-	-	6.5	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	in free air	-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	-	2.5	5	mA
		T2+ G-	-	3.5	5	mA
		T2- G-	-	3.5	5	mA
		T2- G+	-	6.5	10	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	1.6	15	mA
		T2+ G-	-	8.5	20	mA
		T2- G-	-	1.2	15	mA
		T2- G+	-	2.5	20	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	1.5	10	mA
V_T	On-state voltage	I_T = 10 A	-	1.3	1.65	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	$V_D = V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; R_{GK} = 1 kΩ	-	5	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 12 A; $V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs

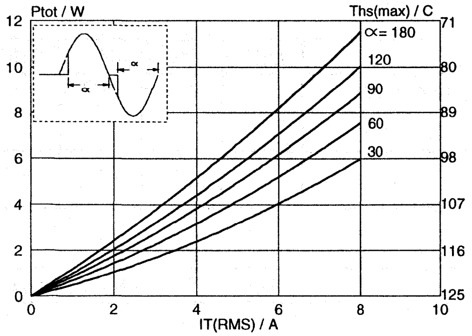


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

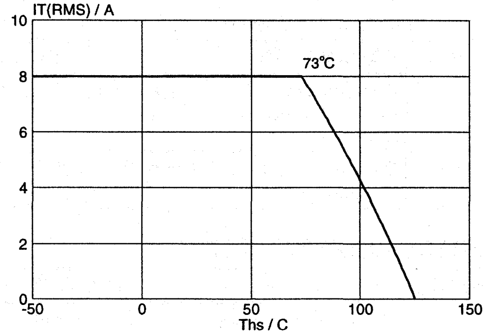


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature T_{hs}.

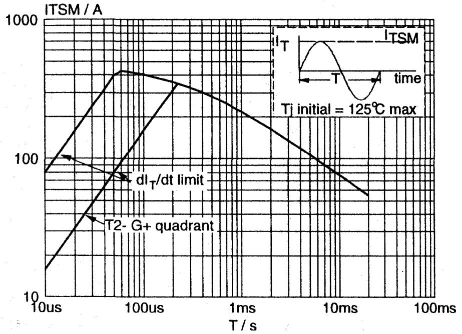


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

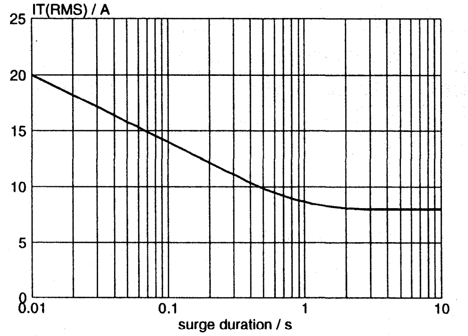


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 73$ °C.

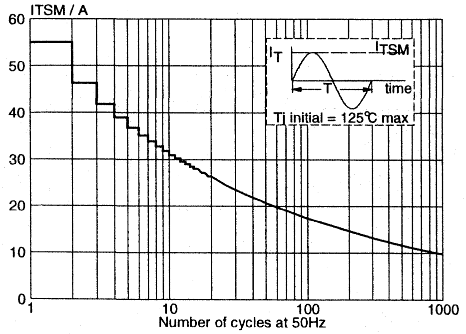


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

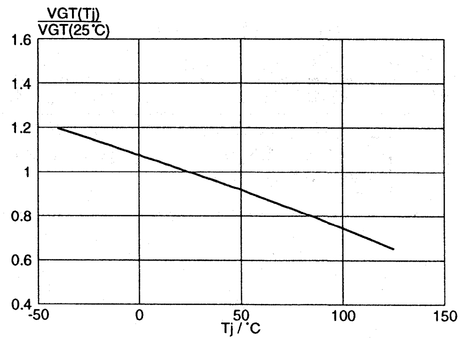


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25$ °C$)$, versus junction temperature T_j.

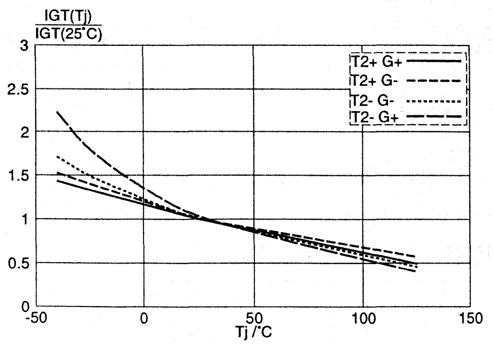


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/I_{GT}(25˚C)$, versus junction temperature T_j.

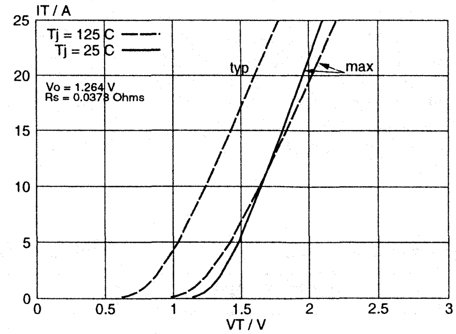


Fig.10. Typical and maximum on-state characteristic.

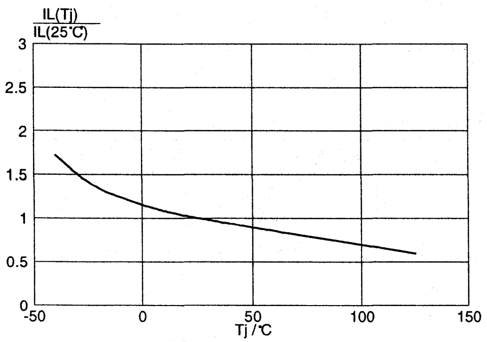


Fig.8. Normalised latching current $I_L(T_j)/I_L(25˚C)$, versus junction temperature T_j.

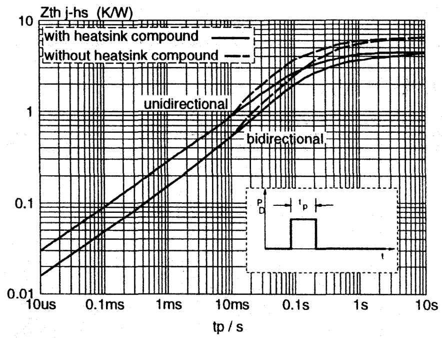


Fig.11. Transient thermal impedance $Z_{th\,j\text{-}hs}$, versus pulse width t_p.

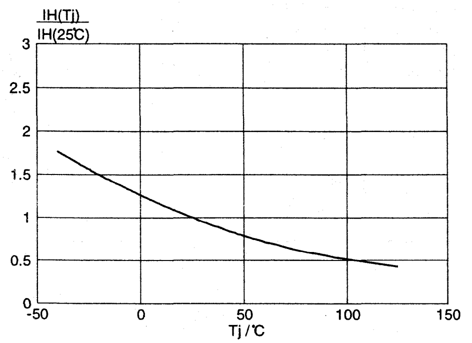


Fig.9. Normalised holding current $I_H(T_j)/I_H(25˚C)$, versus junction temperature T_j.

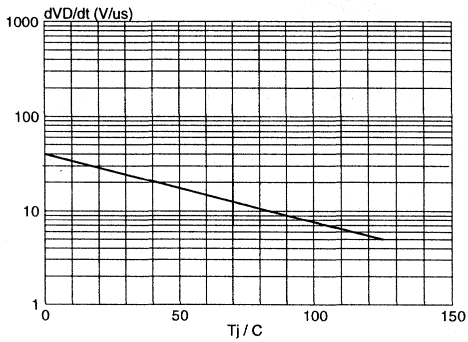


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a full pack, plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

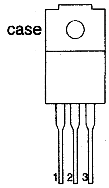
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT137F-	**500E**	**600E**	**800E**	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	8	8	8	A
I_{TSM}	Non-repetitive peak on-state current	55	55	55	A

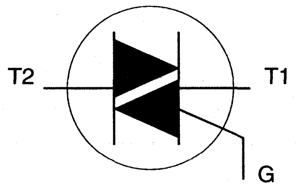
PINNING - SOT186

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	**-600**	**-800**	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{hs} \leq 73$ ˚C	-	8			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 20 ms	-	55			A
		t = 16.7 ms	-	60			A
I^2t	I^2t for fusing	t = 10 ms	-	15			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 12$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs					
		T2+ G+	-	50			A/µs
		T2+ G-	-	50			A/µs
		T2- G-	-	50			A/µs
		T2- G+	-	10			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-hs}$	Thermal resistance junction to heatsink	full or half cycle				
		with heatsink compound	-	-	4.5	K/W
		without heatsink compound	-	-	6.5	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	in free air	-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	-	2.5	10	mA
		T2+ G-	-	4.0	10	mA
		T2- G-	-	5.0	10	mA
		T2- G+	-	11	25	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	3.0	25	mA
		T2+ G-	-	14	35	mA
		T2- G-	-	3.0	25	mA
		T2- G+	-	4.0	35	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	2.5	20	mA
V_T	On-state voltage	I_T = 10 A	-	1.3	1.65	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	-	50	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 12 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs

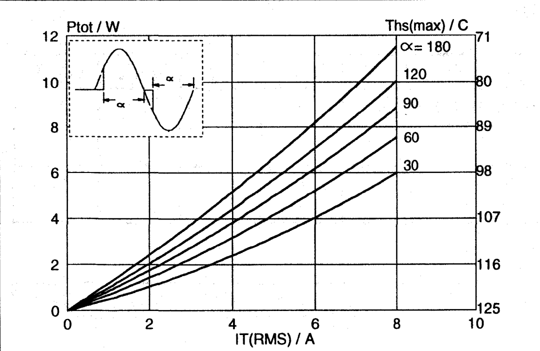


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

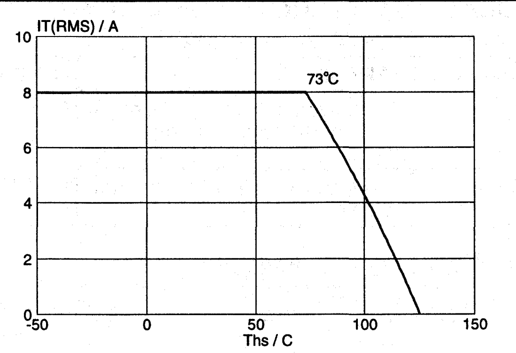


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature T_{hs}.

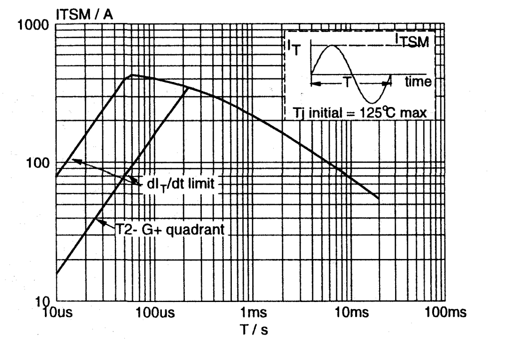


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq$ 20ms.

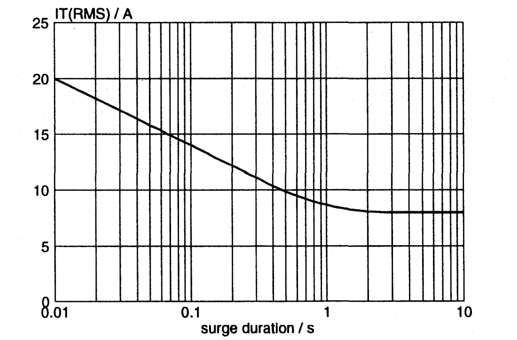


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq$ 73˚C.

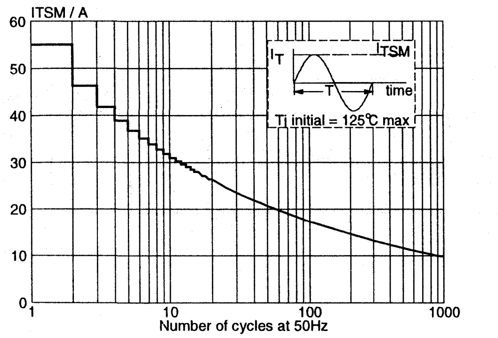


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

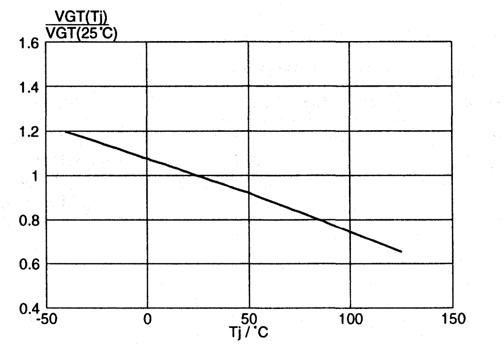


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)$/ V_{GT}(25˚C), versus junction temperature T_j.

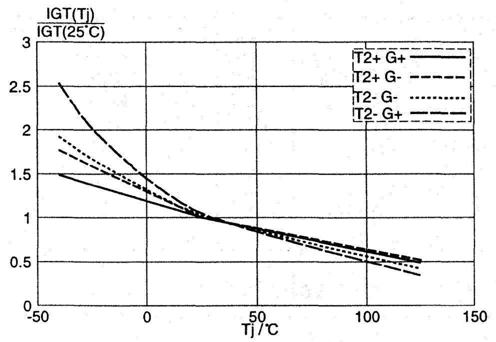


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

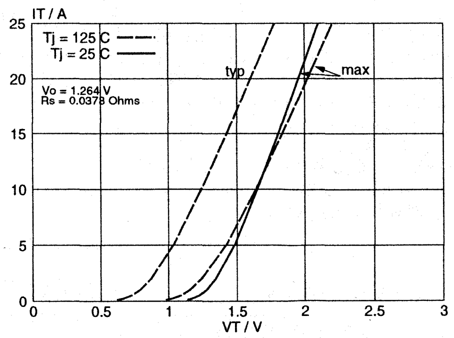


Fig.10. Typical and maximum on-state characteristic.

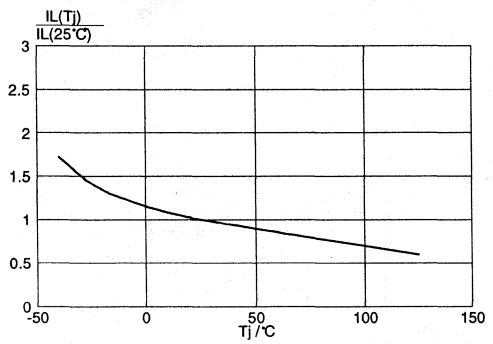


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.

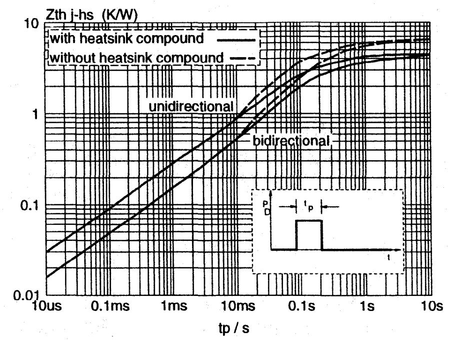


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}hs}$, versus pulse width t_p.

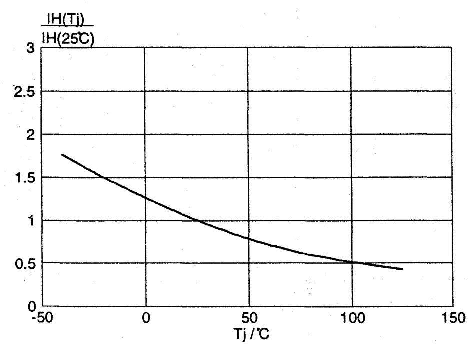


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j.

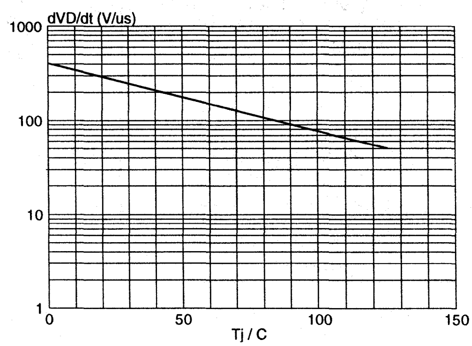


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

GENERAL DESCRIPTION

Glass passivated triacs in a full pack plastic envelope, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

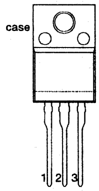
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT137X-	**500**	**600**	**800**	
	BT137X-	**500F**	**600F**	**800F**	
	BT137X-	**500G**	**600G**	**800G**	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	8	8	8	A
I_{TSM}	Non-repetitive peak on-state current	55	55	55	A

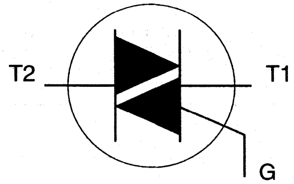
PINNING - SOT186A

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	**-600**	**-800**	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{hs} \leq 73$ ˚C	-	8			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 20 ms	-	55			A
		t = 16.7 ms	-	60			A
I^2t	I^2t for fusing	t = 10 ms	-	15			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 12$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs					
		T2+ G+	-	50			A/µs
		T2+ G-	-	50			A/µs
		T2- G-	-	50			A/µs
		T2- G+	-	10			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-hs}$	Thermal resistance junction to heatsink	full or half cycle				
		with heatsink compound	-	-	4.5	K/W
		without heatsink compound	-	-	6.5	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	in free air	-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.			UNIT
		BT137X-			...	...F	...G	
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A						
		T2+ G+	-	5	35	25	50	mA
		T2+ G-	-	8	35	25	50	mA
		T2- G-	-	11	35	25	50	mA
		T2- G+	-	30	70	70	100	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A						
		T2+ G+	-	7	30	30	45	mA
		T2+ G-	-	16	45	45	60	mA
		T2- G-	-	5	30	30	45	mA
		T2- G+	-	7	45	45	60	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	5	20	20	40	mA
V_T	On-state voltage	I_T = 10 A	-	1.3	1.65			V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5			V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-			V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5			mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.			TYP.	MAX.	UNIT
		BT137X-	...	...F	...G			
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	100	50	200	250	-	V/µs
dV_{com}/dt	Critical rate of change of commutating voltage	V_{DM} = 400 V; T_j = 95 ˚C; $I_{T(RMS)}$ = 8 A; dI_{com}/dt = 3.6 A/ms; gate open circuit	-	-	10	20	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 12 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	-	-	2	-	µs

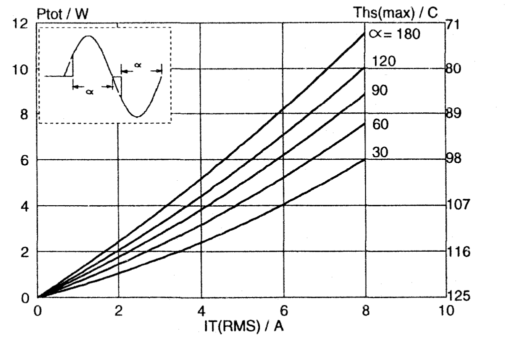


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

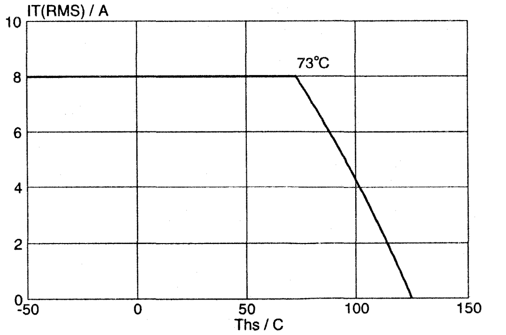


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature T_{hs}.

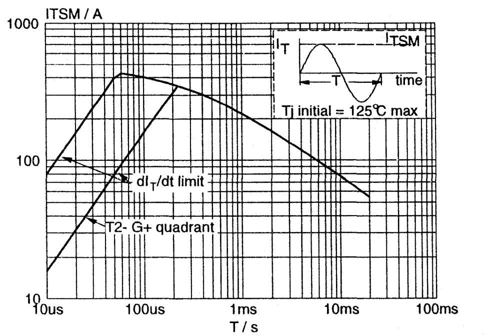


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

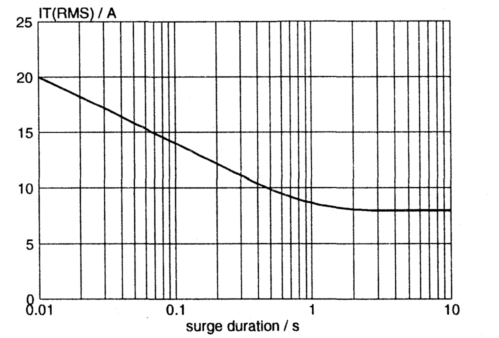


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 73^{\circ}C$.

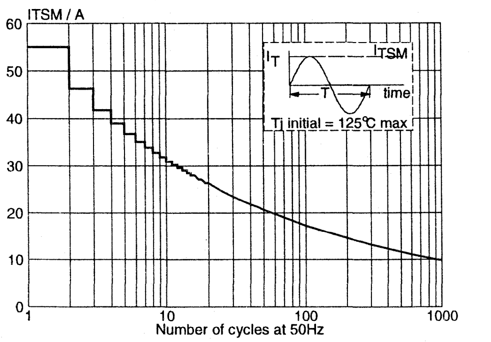


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

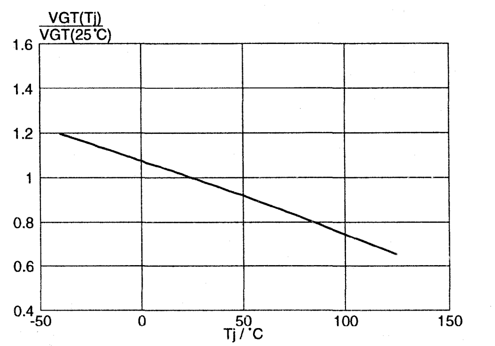


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25^{\circ}C)$, versus junction temperature T_j.

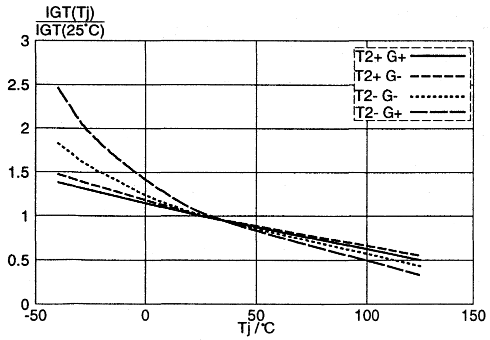


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/\ I_{GT}(25˚C)$, versus junction temperature T_j.

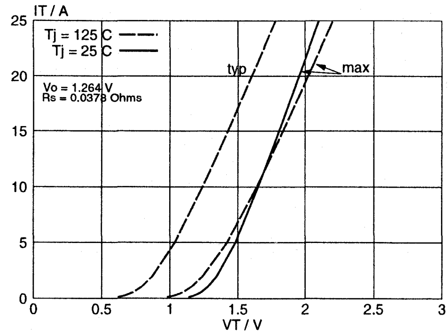


Fig.10. Typical and maximum on-state characteristic.

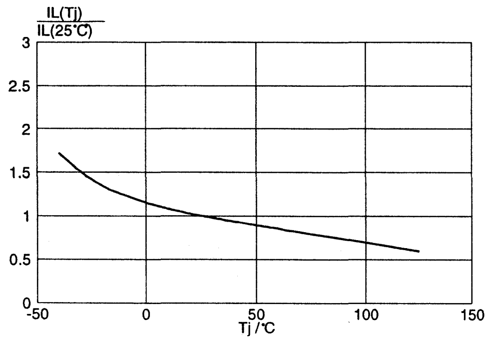


Fig.8. Normalised latching current $I_L(T_j)/\ I_L(25˚C)$, versus junction temperature T_j.

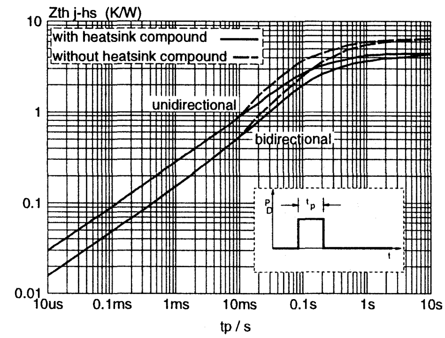


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}hs}$, versus pulse width t_p.

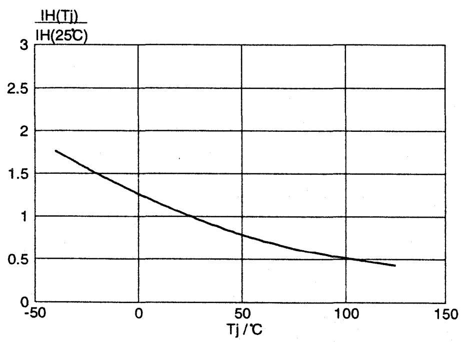


Fig.9. Normalised holding current $I_H(T_j)/\ I_H(25˚C)$, versus junction temperature T_j.

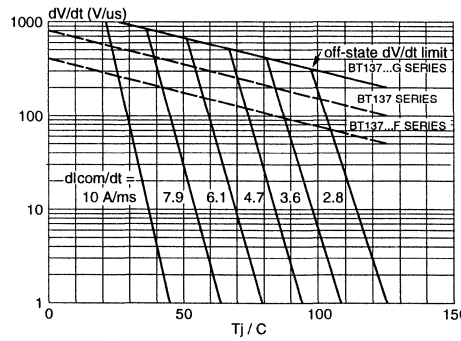


Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation dI_T/dt. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation dI_T/dt.

Triacs logic level

BT137X series D

GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a full pack plastic envelope, intended for use in general purpose bidirectional switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

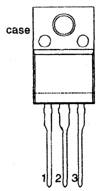
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BT137X-	**500D**	**600D**	
V_{DRM}	Repetitive peak off-state voltages	500	600	V
$I_{T(RMS)}$	RMS on-state current	8	8	A
I_{TSM}	Non-repetitive peak on-state current	55	55	A

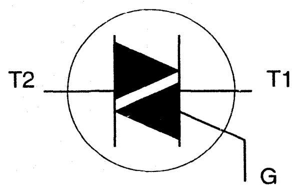
PINNING - SOT186A

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
				-500	**-600**	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{hs} \leq 73$ ˚C	-	8		A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$				
		t = 20 ms	-	55		A
		t = 16.7 ms	-	60		A
I^2t	I^2t for fusing	t = 10 ms	-	15		A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 12$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs				
		T2+ G+	-	50		A/µs
		T2+ G-	-	50		A/µs
		T2- G-	-	50		A/µs
		T2- G+	-	10		A/µs
I_{GM}	Peak gate current		-	2		A
V_{GM}	Peak gate voltage		-	5		V
P_{GM}	Peak gate power		-	5		W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5		W
T_{stg}	Storage temperature		-40	150		˚C
T_j	Operating junction temperature		-	125		˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	full or half cycle with heatsink compound	-	-	4.5	K/W
		without heatsink compound	-	-	6.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	-	2.5	5	mA
		T2+ G-	-	3.5	5	mA
		T2- G-	-	3.5	5	mA
		T2- G+	-	6.5	10	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	1.6	15	mA
		T2+ G-	-	8.5	20	mA
		T2- G-	-	1.2	15	mA
		T2- G+	-	2.5	20	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	1.5	10	mA
V_T	On-state voltage	I_T = 10 A	-	1.3	1.65	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; R_{GK} = 1 kΩ	-	5	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 12 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs

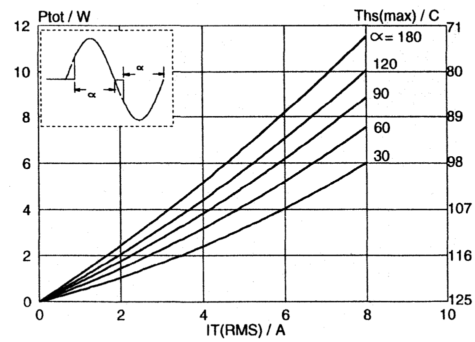


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

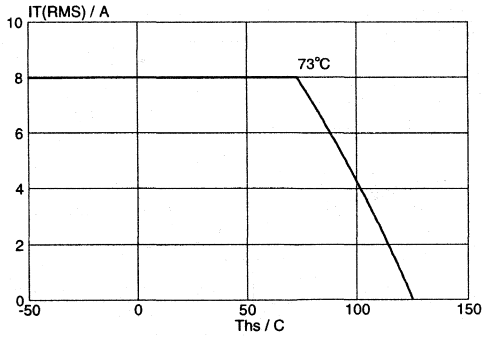


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature T_{hs}.

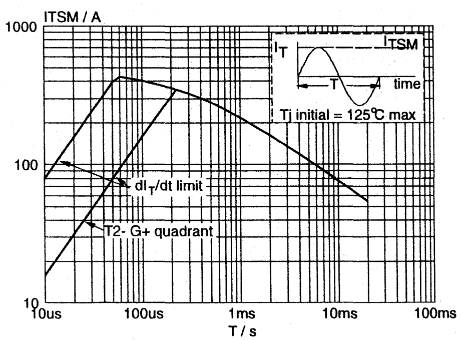


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20$ms.

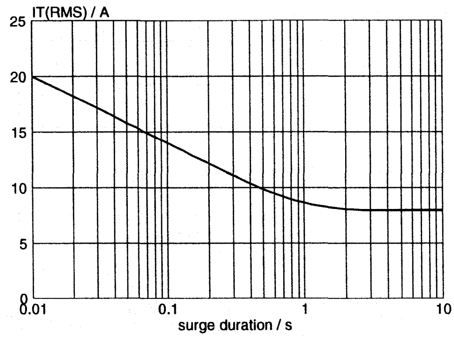


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 73$°C.

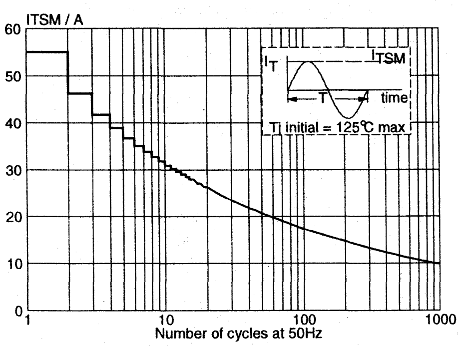


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

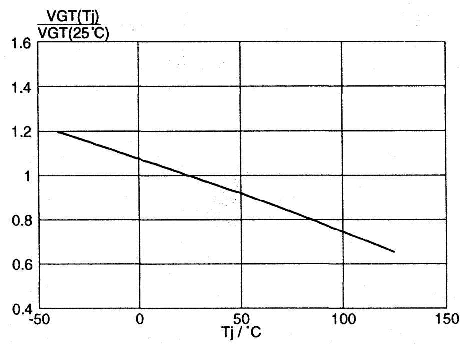


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25°C)$, versus junction temperature T_j.

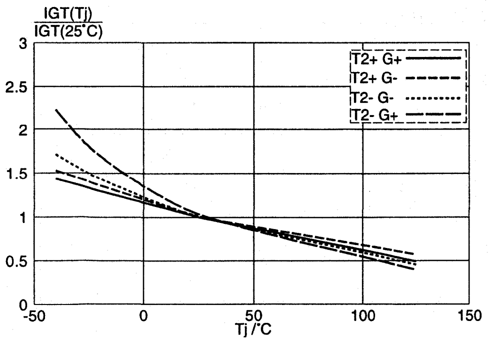


Fig.7. Normalised gate trigger current $I_{GT}(T_j)$/ $I_{GT}(25˚C)$, versus junction temperature T_j.

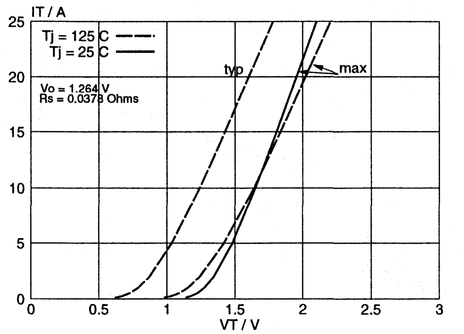


Fig.10. Typical and maximum on-state characteristic.

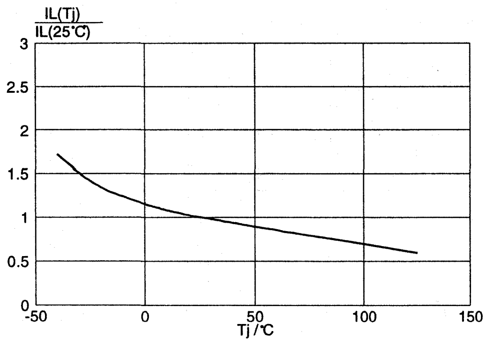


Fig.8. Normalised latching current $I_L(T_j)$/ $I_L(25˚C)$, versus junction temperature T_j.

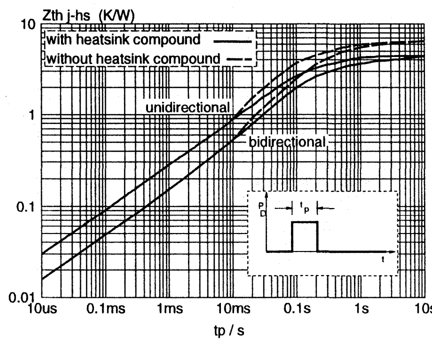


Fig.11. Transient thermal impedance $Z_{th\ j-hs}$, versus pulse width t_p.

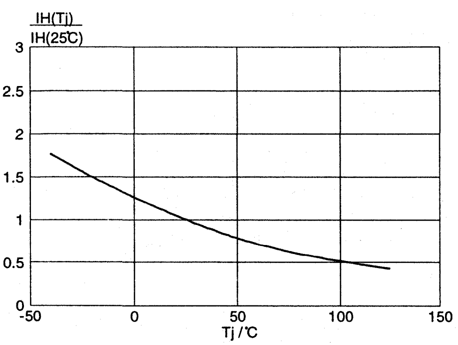


Fig.9. Normalised holding current $I_H(T_j)$/ $I_H(25˚C)$, versus junction temperature T_j.

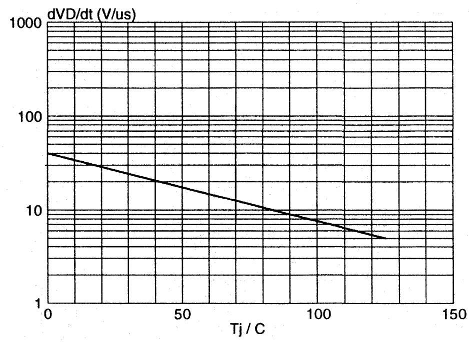


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a full pack, plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

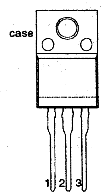
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT137X-	500E	600E	800E	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	8	8	8	A
I_{TSM}	Non-repetitive peak on-state current	55	55	55	A

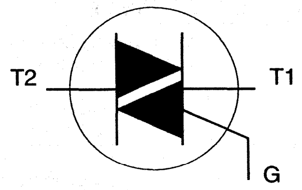
PINNING - SOT186A

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	-600	-800	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{hs} \leq 73$ ˚C	-	8			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 20 ms	-	55			A
		t = 16.7 ms	-	60			A
I^2t	I^2t for fusing	t = 10 ms	-	15			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 12$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs					
		T2+ G+	-	50			A/µs
		T2+ G-	-	50			A/µs
		T2- G-	-	50			A/µs
		T2- G+	-	10			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-hs}$	Thermal resistance junction to heatsink	full or half cycle				
		with heatsink compound	-	-	4.5	K/W
		without heatsink compound	-	-	6.5	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	in free air	-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	-	2.5	10	mA
		T2+ G-	-	4.0	10	mA
		T2- G-	-	5.0	10	mA
		T2- G+	-	11	25	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	3.0	25	mA
		T2+ G-	-	14	35	mA
		T2- G-	-	3.0	25	mA
		T2- G+	-	4.0	35	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	2.5	20	mA
V_T	On-state voltage	I_T = 10 A	-	1.3	1.65	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	-	50	-	V/µs
t_{gt}	Gate controlled turn-on time	V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs; I_{TM} = 12 A	-	2	-	µs

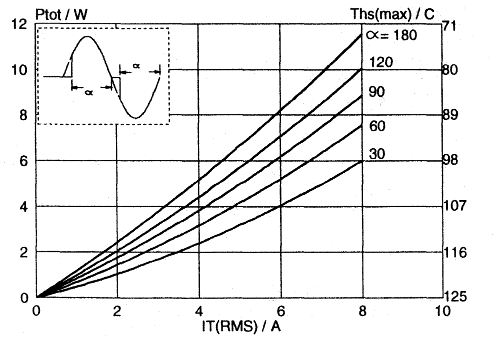


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

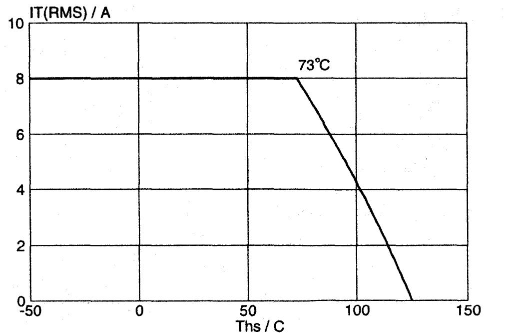


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature T_{hs}.

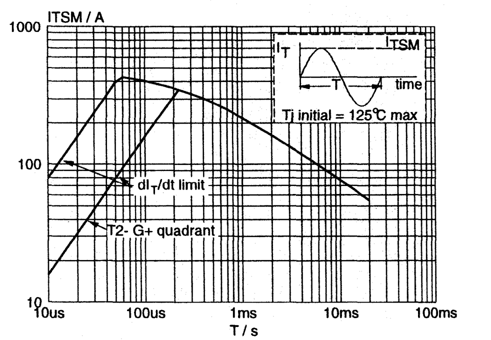


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20$ms.

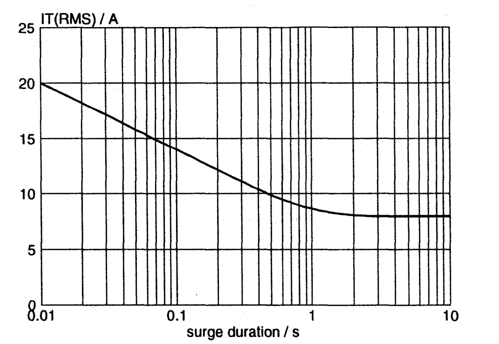


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 73$˚C.

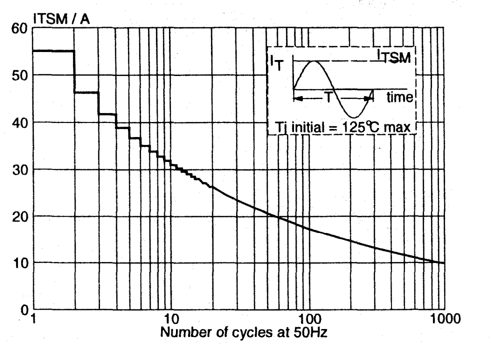


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

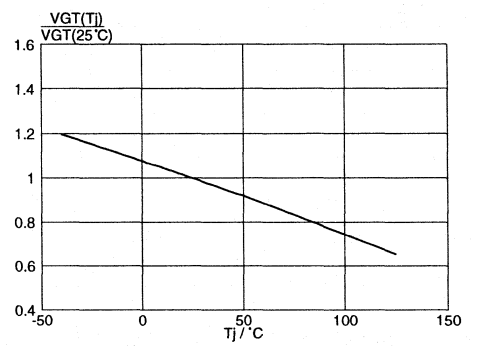


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25˚C)$, versus junction temperature T_j.

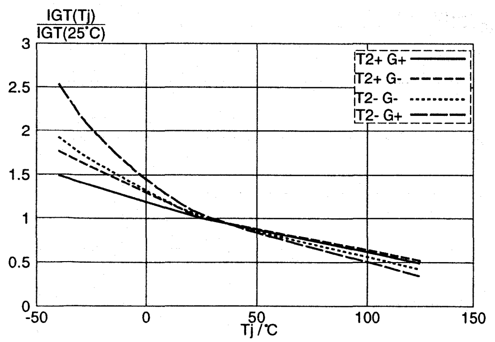


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

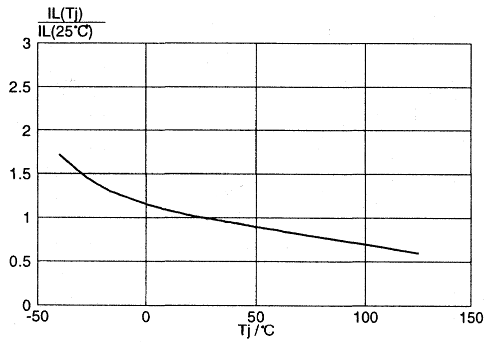


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.

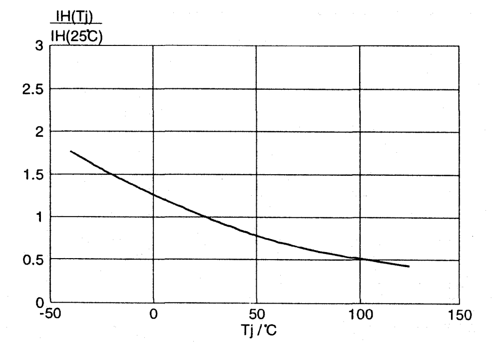


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j.

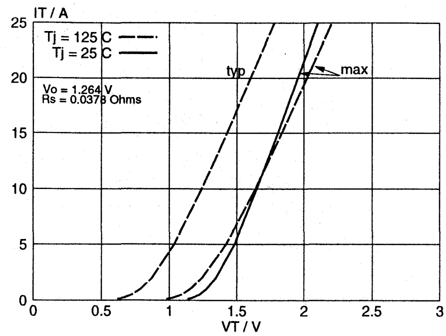


Fig.10. Typical and maximum on-state characteristic.

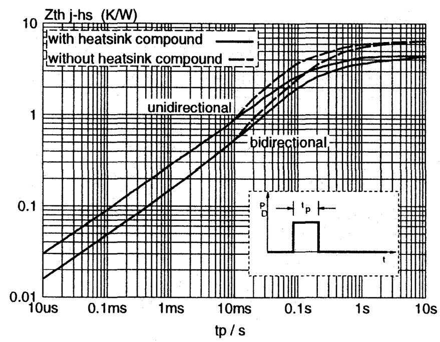


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}hs}$, versus pulse width t_p.

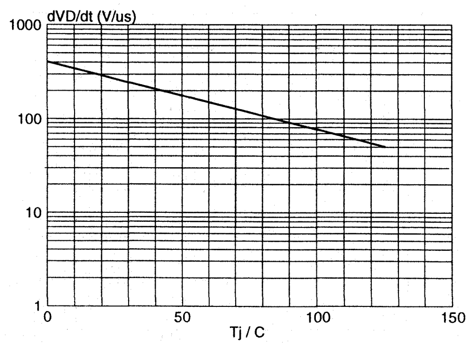


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

GENERAL DESCRIPTION

Glass passivated triacs in a plastic envelope, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

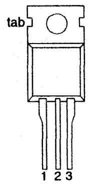
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT138-	**500**	**600**	**800**	
	BT138-	**500F**	**600F**	**800F**	
	BT138-	**500G**	**600G**	**800G**	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	12	12	12	A
I_{TSM}	Non-repetitive peak on-state current	90	90	90	A

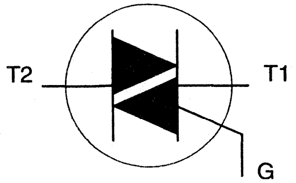
PINNING - TO220AB

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
tab	main terminal 2

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	**-600**	**-800**	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 99$ ˚C	-	12			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 20 ms	-	90			A
		t = 16.7 ms	-	100			A
I^2t	I^2t for fusing	t = 10 ms	-	40			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs					
		T2+ G+	-	50			A/µs
		T2+ G-	-	50			A/µs
		T2- G-	-	50			A/µs
		T2- G+	-	10			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	full cycle	-	-	1.5	K/W
		half cycle	-	-	2.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.			UNIT
		BT138-			...	...F	...G	
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A						
		T2+ G+	-	5	35	25	50	mA
		T2+ G-	-	8	35	25	50	mA
		T2- G-	-	10	35	25	50	mA
		T2- G+	-	22	70	70	100	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A						
		T2+ G+	-	7	40	40	60	mA
		T2+ G-	-	20	60	60	90	mA
		T2- G-	-	8	40	40	60	mA
		T2- G+	-	10	60	60	90	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	6	30	30	60	mA
V_T	On-state voltage	I_T = 15 A	-	1.4	1.65			V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5			V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-			V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5			mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.			TYP.	MAX.	UNIT
		BT138-	...	...F	...G			
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	100	50	200	250	-	V/µs
dV_{com}/dt	Critical rate of change of commutating voltage	V_{DM} = 400 V; T_j = 95 ˚C; $I_{T(RMS)}$ = 12 A; dI_{com}/dt = 5.4 A/ms; gate open circuit	-	-	10	20	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 16 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	-	-	2	-	µs

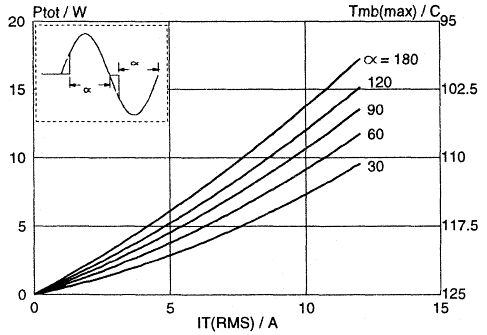


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

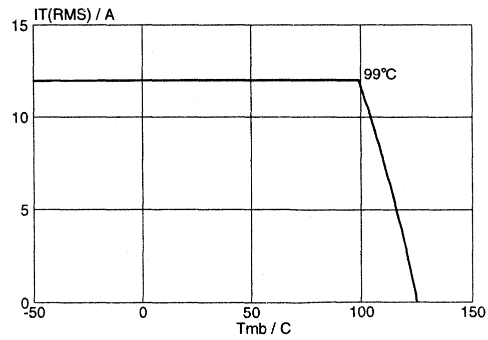


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

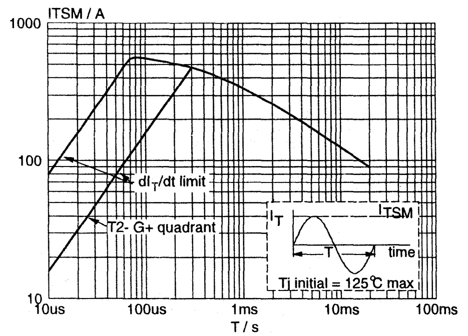


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

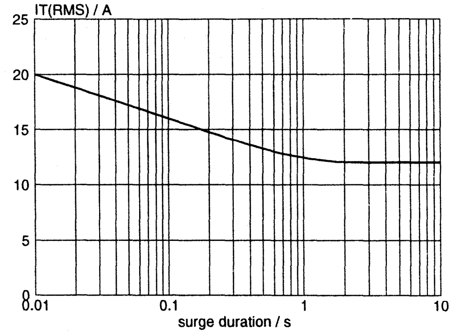


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 99^{\circ}C$.

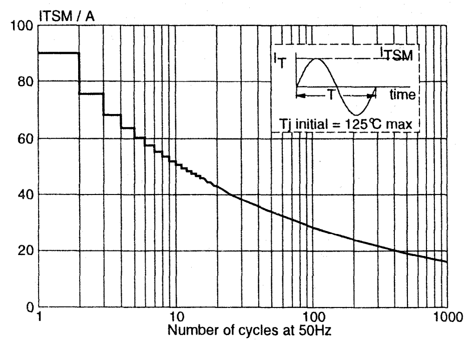


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

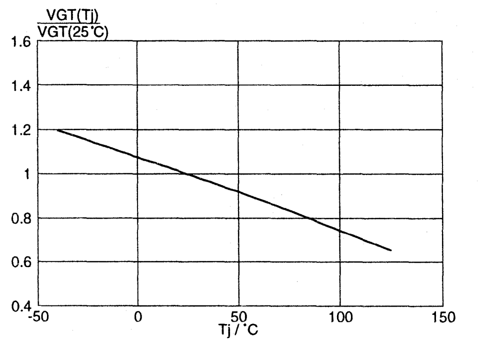


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25^{\circ}C)$, versus junction temperature T_j.

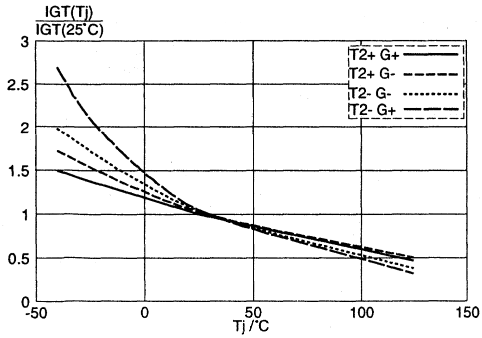


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/I_{GT}(25°C)$, versus junction temperature T_j.

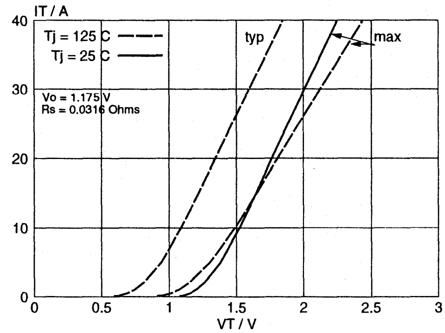


Fig.10. Typical and maximum on-state characteristic.

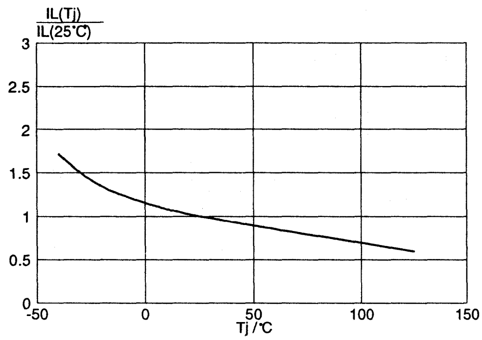


Fig.8. Normalised latching current $I_L(T_j)/I_L(25°C)$, versus junction temperature T_j.

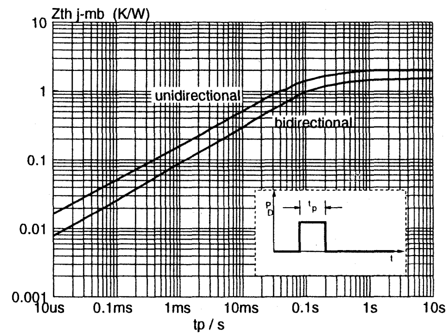


Fig.11. Transient thermal impedance $Z_{th\,j\text{-}mb}$, versus pulse width t_p.

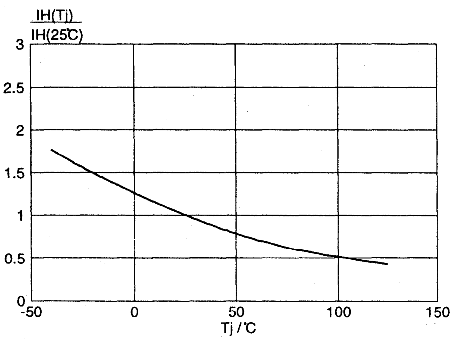


Fig.9. Normalised holding current $I_H(T_j)/I_H(25°C)$, versus junction temperature T_j.

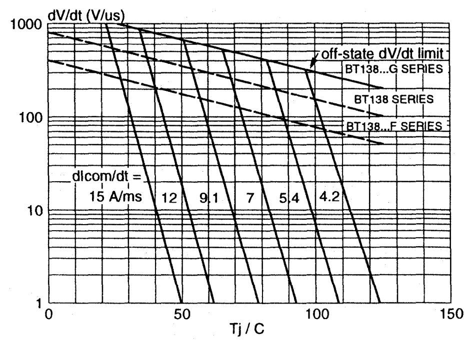


Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation dI_T/dt. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation dI_T/dt.

GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

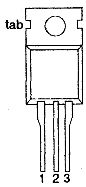
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT138-	**500E**	**600E**	**800E**	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	12	12	12	A
I_{TSM}	Non-repetitive peak on-state current	90	90	90	A

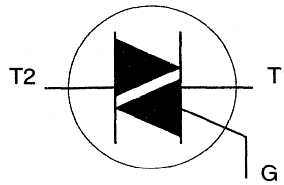
PINNING - TO220AB

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
tab	main terminal 2

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	**-600**	**-800**	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 99$ ˚C	-	12			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 20 ms	-	90			A
		t = 16.7 ms	-	100			A
I^2t	I^2t for fusing	t = 10 ms	-	40			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs					
		T2+ G+	-	50			A/µs
		T2+ G-	-	50			A/µs
		T2- G-	-	50			A/µs
		T2- G+	-	10			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	full cycle	-	-	1.5	K/W
		half cycle	-	-	2.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	-	2.5	10	mA
		T2+ G-	-	4.0	10	mA
		T2- G-	-	5.0	10	mA
		T2- G+	-	11	25	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	3.2	30	mA
		T2+ G-	-	16	40	mA
		T2- G-	-	4.0	30	mA
		T2- G+	-	5.5	40	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	4.0	30	mA
V_T	On-state voltage	I_T = 15 A	-	1.4	1.65	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	$V_D = V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	-	50	-	V/μs
t_{gt}	Gate controlled turn-on time	I_{TM} = 16 A; $V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/μs	-	2	-	μs

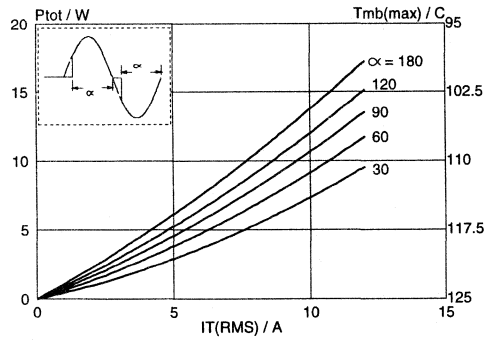


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

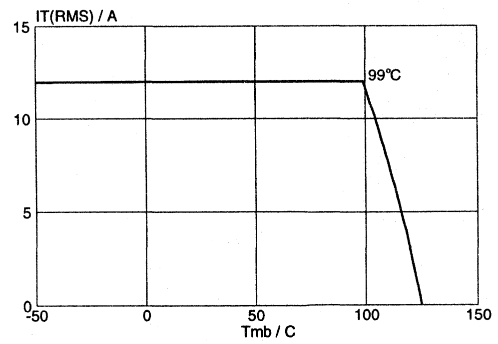


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

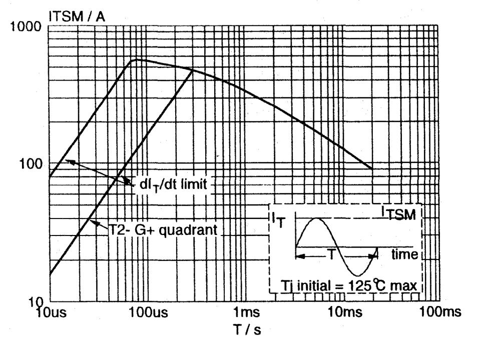


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq$ 20ms.

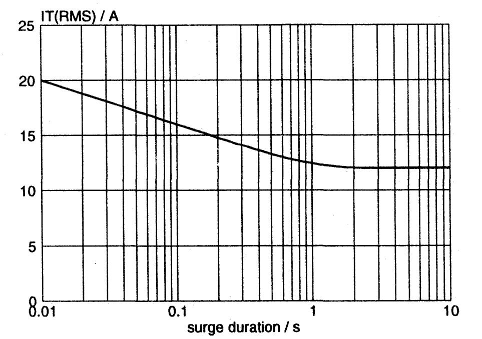


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq$ 99˚C.

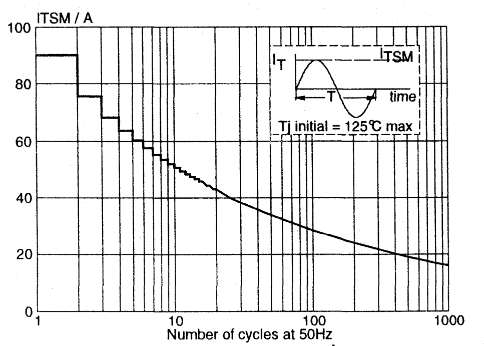


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

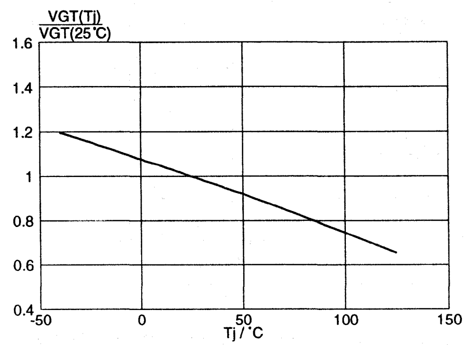


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)$/ V_{GT}(25˚C), versus junction temperature T_j.

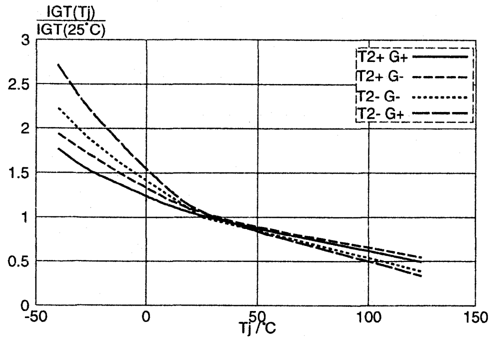


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

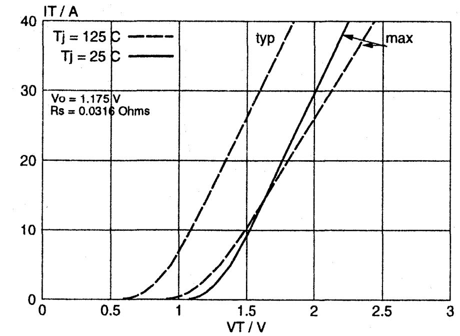


Fig.10. Typical and maximum on-state characteristic.

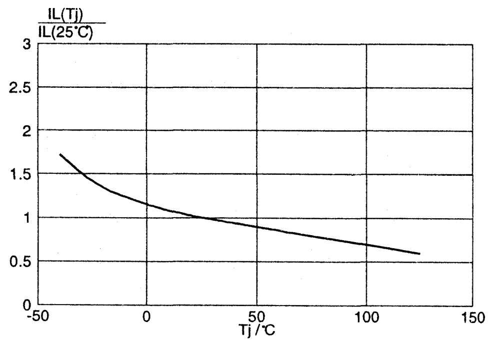


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.

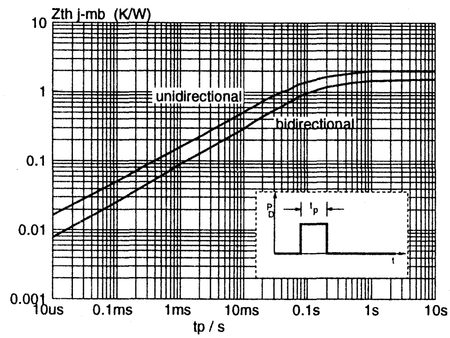


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width t_p.

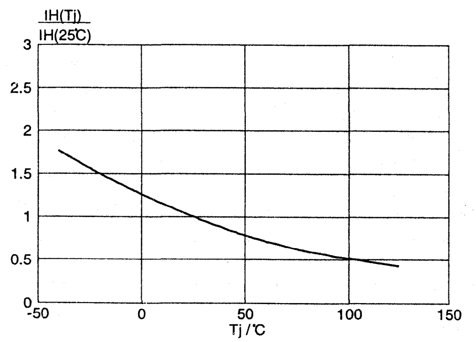


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j.

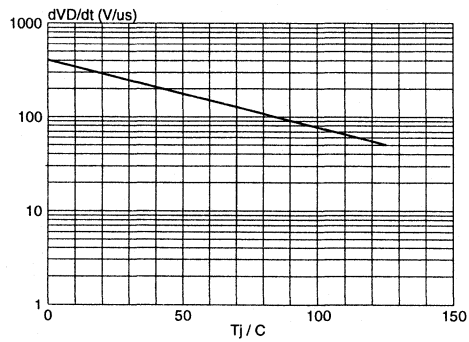


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

GENERAL DESCRIPTION

Glass passivated triacs in a full pack plastic envelope, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

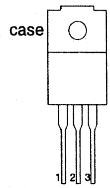
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT138F-	**500**	**600**	**800**	
	BT138F-	**500F**	**600F**	**800F**	
	BT138F-	**500G**	**600G**	**800G**	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	12	12	12	A
I_{TSM}	Non-repetitive peak on-state current	90	90	90	A

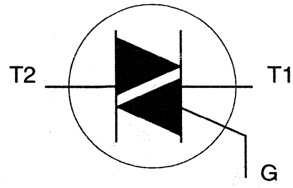
PINNING - SOT186

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	**-600**	**-800**	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{hs} \leq 56$ ˚C	-	12			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 20 ms	-	90			A
		t = 16.7 ms	-	100			A
I^2t	I^2t for fusing	t = 10 ms	-	40			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs					
		T2+ G+	-	50			A/µs
		T2+ G-	-	50			A/µs
		T2- G-	-	50			A/µs
		T2- G+	-	10			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-hs}$	Thermal resistance junction to heatsink	full or half cycle				
		with heatsink compound	-	-	4.0	K/W
		without heatsink compound	-	-	5.5	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	in free air	-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.			UNIT
		BT138F-			...	...F	...G	
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A						
		T2+ G+	-	5	35	25	50	mA
		T2+ G-	-	8	35	25	50	mA
		T2- G-	-	10	35	25	50	mA
		T2- G+	-	22	70	70	100	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A						
		T2+ G+	-	7	40	40	60	mA
		T2+ G-	-	20	60	60	90	mA
		T2- G-	-	8	40	40	60	mA
		T2- G+	-	10	60	60	90	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	6	30	30	60	mA
V_T	On-state voltage	I_T = 15 A	-	1.4	1.65			V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5			V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-			V
I_D	Off-state leakage current	$V_D = V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5			mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.			TYP.	MAX.	UNIT
		BT138F-	...	...F	...G			
dV_D/dt	Critical rate of change of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	100	50	200	250	-	V/μs
dV_{com}/dt	Critical rate of change of commutating voltage	V_{DM} = 400 V; T_j = 95 ˚C; $I_{T(RMS)}$ = 12 A; dI_{com}/dt = 5.4 A/ms; gate open circuit	-	-	10	20	-	V/μs
t_{gt}	Gate controlled turn-on time	I_{TM} = 16 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/μs	-	-	-	2	-	μs

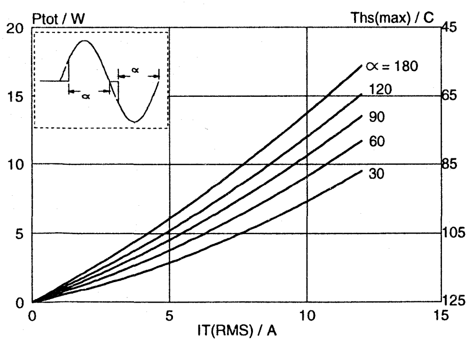


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

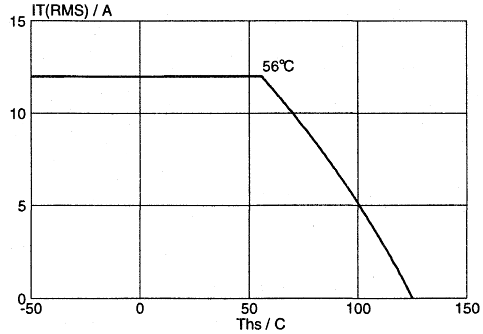


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature T_{hs}.

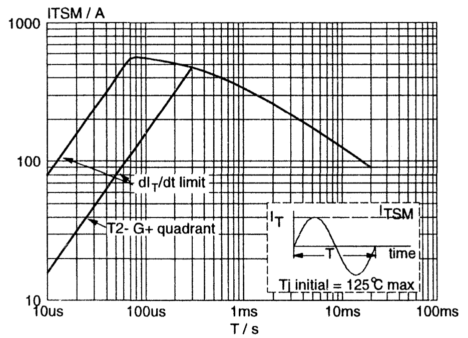


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \le 20$ms.

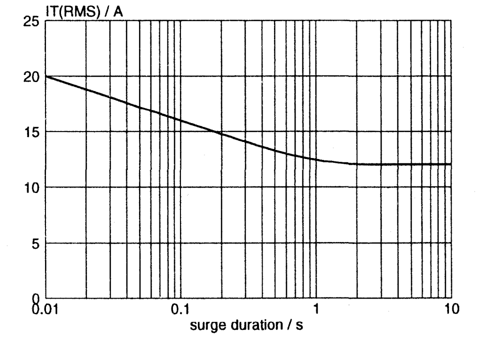


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \le 56$°C.

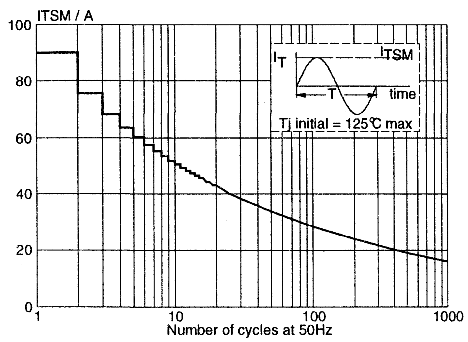


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

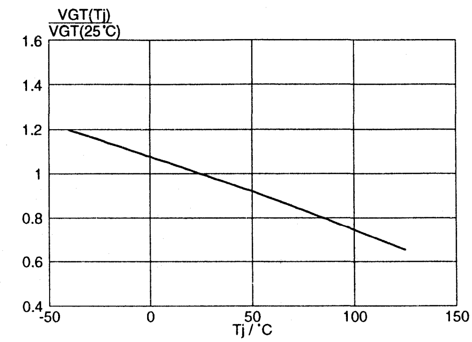


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25°C)$, versus junction temperature T_j.

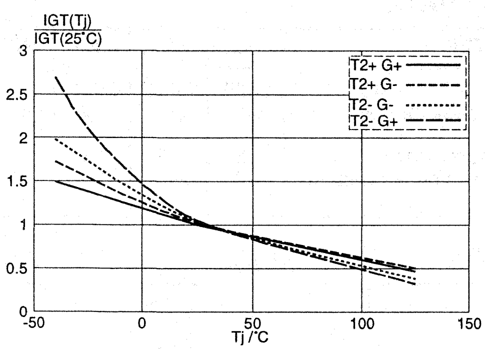


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

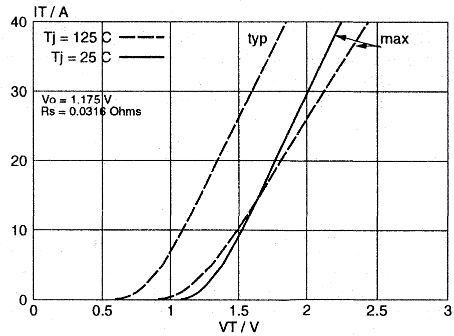


Fig.10. Typical and maximum on-state characteristic.

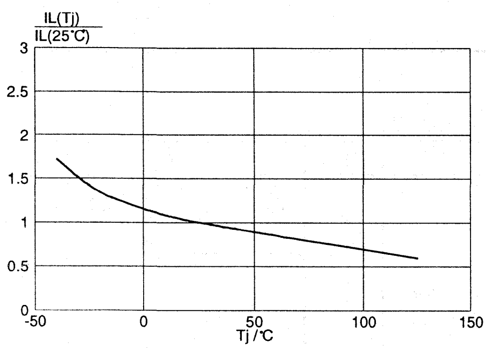


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.

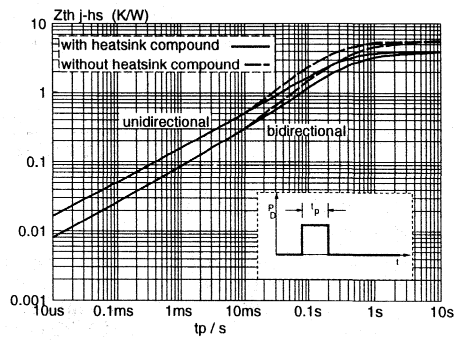


Fig.11. Transient thermal impedance $Z_{th\,j\text{-}hs}$, versus pulse width t_p.

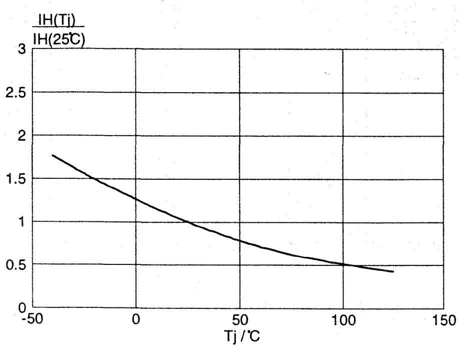


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j.

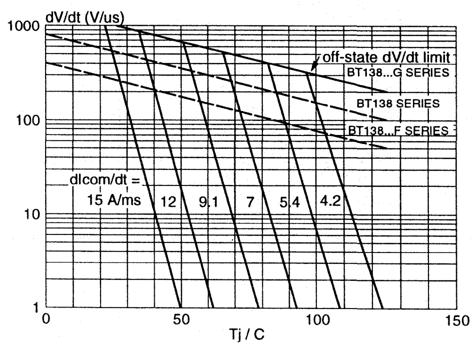


Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation dI_T/dt. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation dI_T/dt.

Triacs sensitive gate

BT138F series E

GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a full pack plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

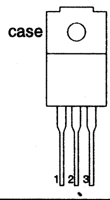
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT138F-	500E	600E	800E	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	12	12	12	A
I_{TSM}	Non-repetitive peak on-state current	90	90	90	A

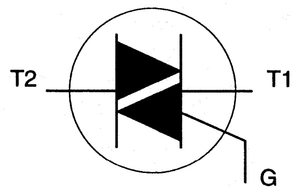
PINNING - SOT186

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	-600	-800	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{hs} \leq 56$ ˚C	-	12			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 20 ms	-	90			A
		t = 16.7 ms	-	100			A
I^2t	I^2t for fusing	t = 10 ms	-	40			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs					
		T2+ G+	-	50			A/µs
		T2+ G-	-	50			A/µs
		T2- G-	-	50			A/µs
		T2- G+	-	10			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-hs}$	Thermal resistance junction to heatsink	full or half cycle with heatsink compound without heatsink compound	 - -	 - -	 4.0 5.5	 K/W K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	in free air	-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	-	2.5	10	mA
		T2+ G-	-	4.0	10	mA
		T2- G-	-	5.0	10	mA
		T2- G+	-	11	25	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	3.2	30	mA
		T2+ G-	-	16	40	mA
		T2- G-	-	4.0	30	mA
		T2- G+	-	5.5	40	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	4.0	30	mA
V_T	On-state voltage	I_T = 15 A	-	1.4	1.65	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	-	50	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 16 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs

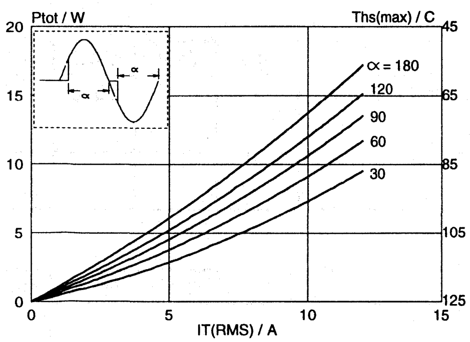


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

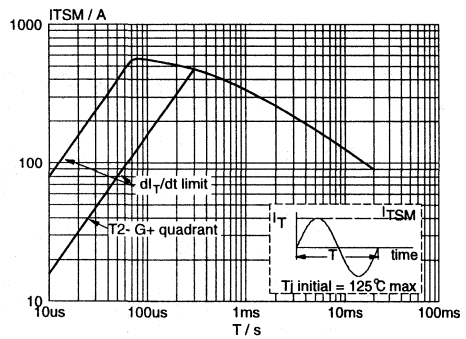


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

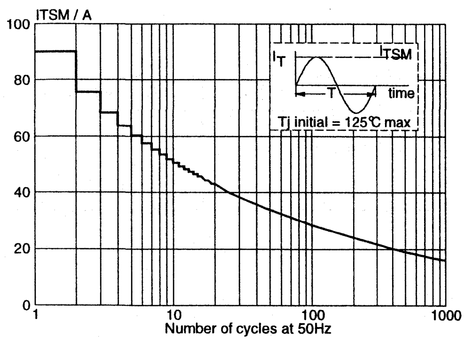


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

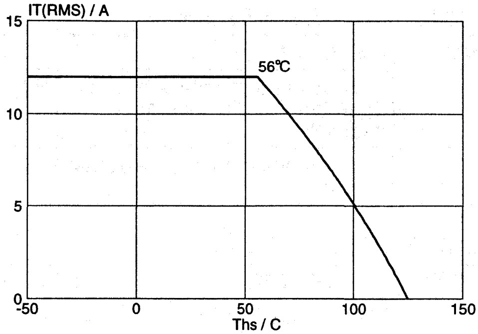


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature T_{hs}.

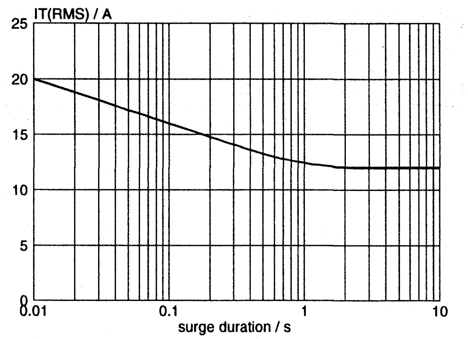


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 56$°C.

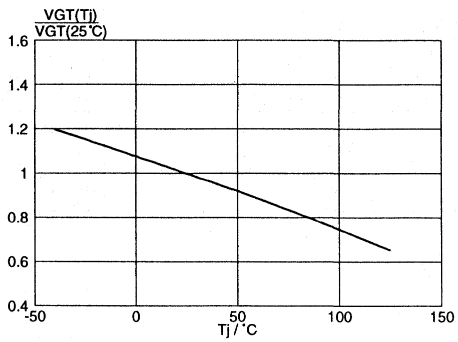


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25°C)$, versus junction temperature T_j.

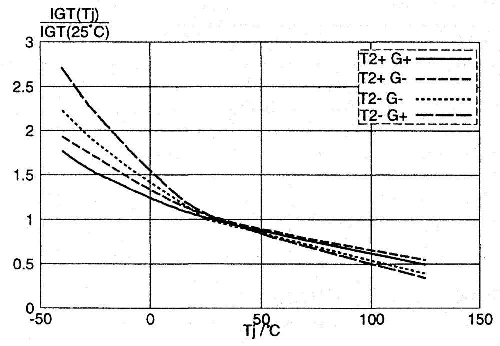


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

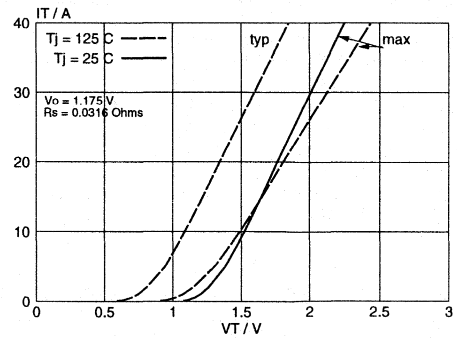


Fig.10. Typical and maximum on-state characteristic.

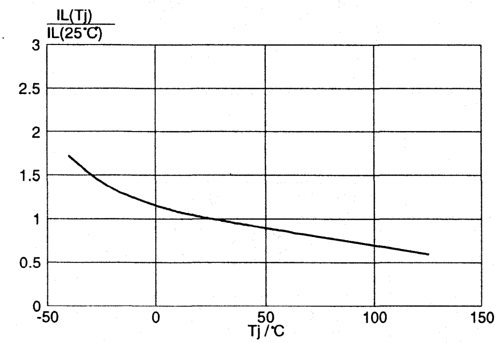


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.

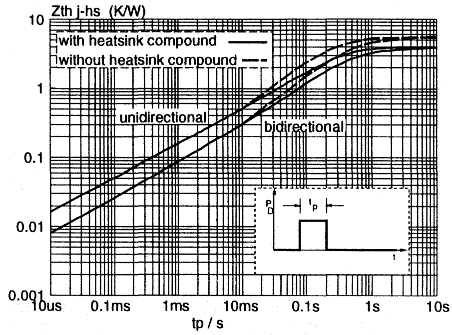


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}hs}$, versus pulse width t_p.

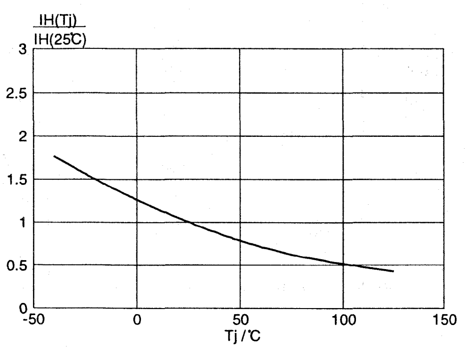


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j.

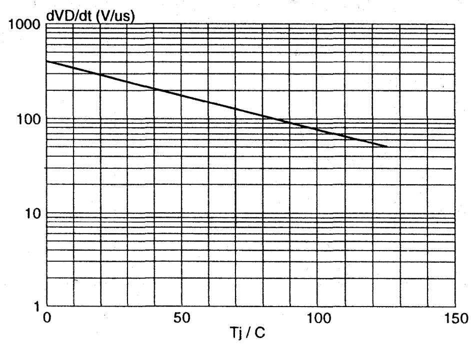


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

GENERAL DESCRIPTION

Glass passivated triacs in a full pack plastic envelope, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

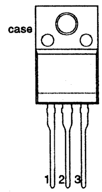
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT138X-	**500**	**600**	**800**	
	BT138X-	**500F**	**600F**	**800F**	
	BT138X-	**500G**	**600G**	**800G**	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	12	12	12	A
I_{TSM}	Non-repetitive peak on-state current	90	90	90	A

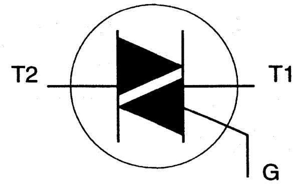
PINNING - SOT186A

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	**-600**	**-800**	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{hs} \leq 56$ ˚C	-	12			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 20 ms	-	90			A
		t = 16.7 ms	-	100			A
I^2t	I^2t for fusing	t = 10 ms	-	40			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs					
		T2+ G+	-	50			A/µs
		T2+ G-	-	50			A/µs
		T2- G-	-	50			A/µs
		T2- G+	-	10			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	full or half cycle				
		with heatsink compound	-	-	4.0	K/W
		without heatsink compound	-	-	5.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.			UNIT
		BT138X-			...	...F	...G	
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A						
		T2+ G+	-	5	35	25	50	mA
		T2+ G-	-	8	35	25	50	mA
		T2- G-	-	10	35	25	50	mA
		T2- G+	-	22	70	70	100	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A						
		T2+ G+	-	7	40	40	60	mA
		T2+ G-	-	20	60	60	90	mA
		T2- G-	-	8	40	40	60	mA
		T2- G+	-	10	60	60	90	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	6	30	30	60	mA
V_T	On-state voltage	I_T = 15 A	-	1.4	1.65			V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5			V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-			V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5			mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.			TYP.	MAX.	UNIT
		BT138X-	...	...F	...G			
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	100	50	200	250	-	V/µs
dV_{com}/dt	Critical rate of change of commutating voltage	V_{DM} = 400 V; T_j = 95 ˚C; $I_{T(RMS)}$ = 12 A; dI_{com}/dt = 5.4 A/ms; gate open circuit	-	-	10	20	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 16 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	-	-	2	-	µs

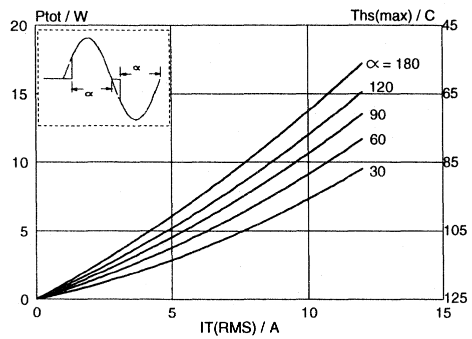


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

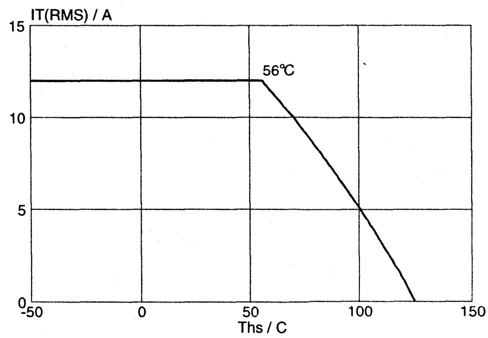


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature T_{hs}.

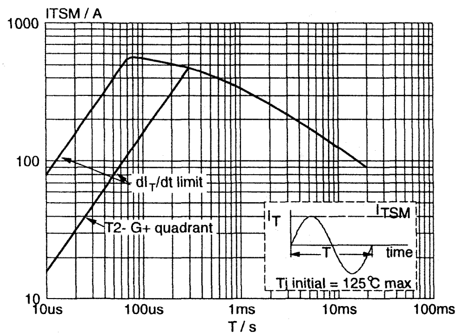


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20$ms.

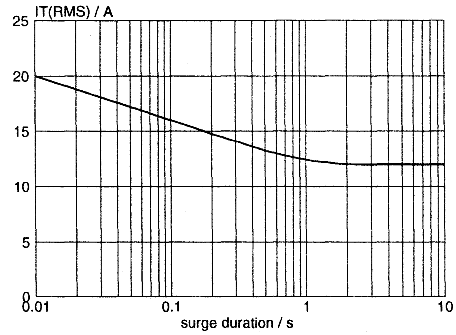


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 56$˚C.

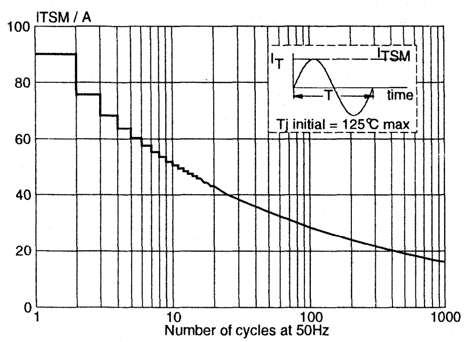


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

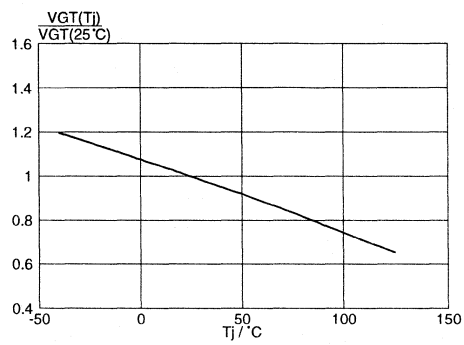


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)$/ $V_{GT}(25˚C)$, versus junction temperature T_j.

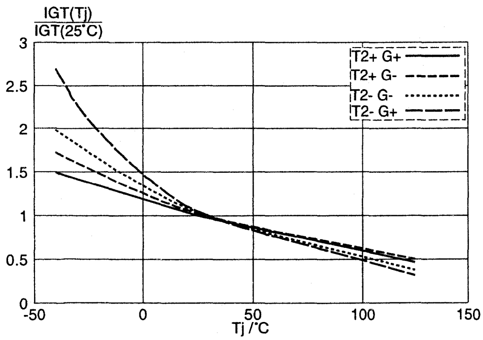


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

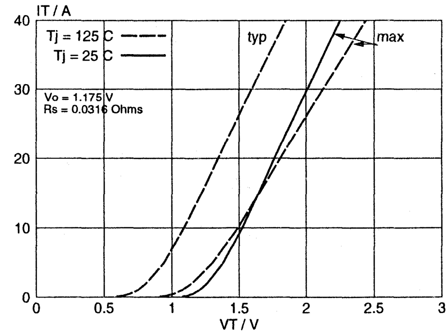


Fig.10. Typical and maximum on-state characteristic.

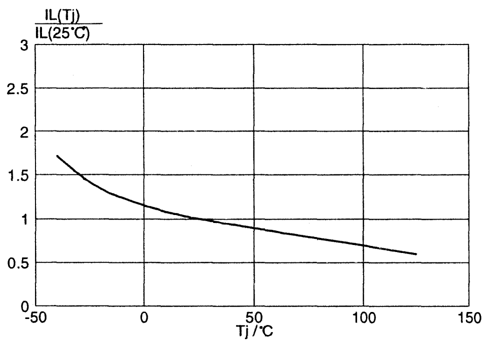


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.

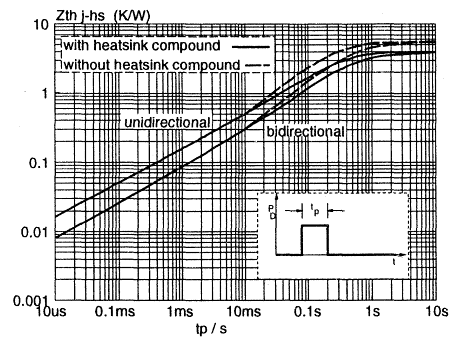


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}hs}$, versus pulse width t_p.

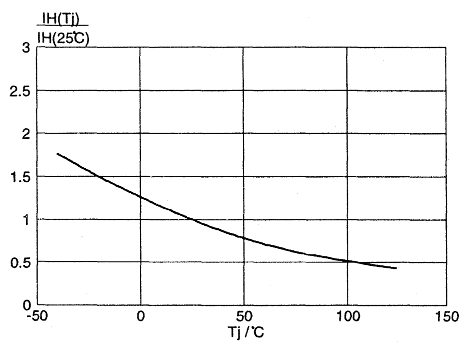


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j.

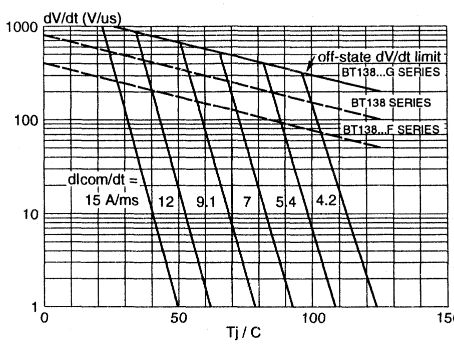


Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation dI_T/dt. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation dI_T/dt.

Triacs sensitive gate

BT138X series E

GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a full pack plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

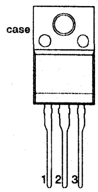
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT138X-	500E	600E	800E	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	12	12	12	A
I_{TSM}	Non-repetitive peak on-state current	90	90	90	A

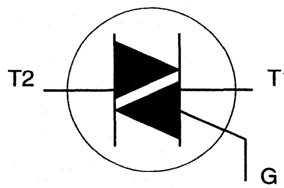
PINNING - SOT186A

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX. -500	MAX. -600	MAX. -800	UNIT
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{hs} \leq 56$ ˚C	-	12			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 20 ms	-	90			A
		t = 16.7 ms	-	100			A
I^2t	I^2t for fusing	t = 10 ms	-	40			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs					
		T2+ G+	-	50			A/µs
		T2+ G-	-	50			A/µs
		T2- G-	-	50			A/µs
		T2- G+	-	10			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-hs}$	Thermal resistance junction to heatsink	full or half cycle				
		with heatsink compound	-	-	4.0	K/W
		without heatsink compound	-	-	5.5	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	in free air	-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	-	2.5	10	mA
		T2+ G-	-	4.0	10	mA
		T2- G-	-	5.0	10	mA
		T2- G+	-	11	25	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	3.2	30	mA
		T2+ G-	-	16	40	mA
		T2- G-	-	4.0	30	mA
		T2- G+	-	5.5	40	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	4.0	30	mA
V_T	On-state voltage	I_T = 15 A	-	1.4	1.65	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	-	50	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 16 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs

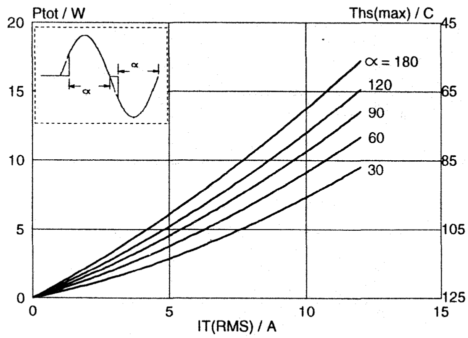


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

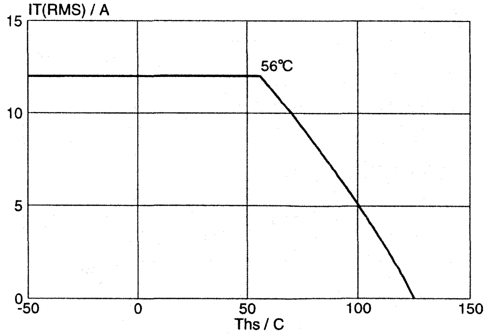


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature T_{hs}.

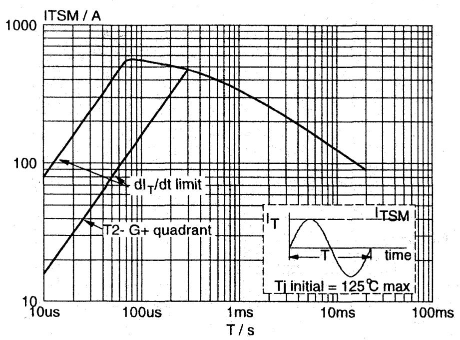


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

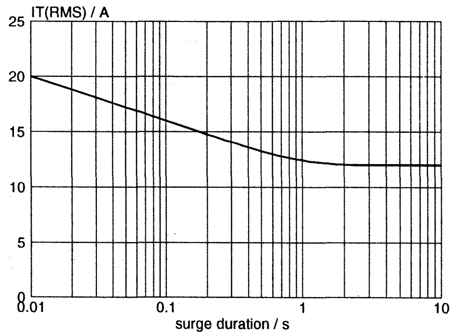


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 56^{\circ}C$.

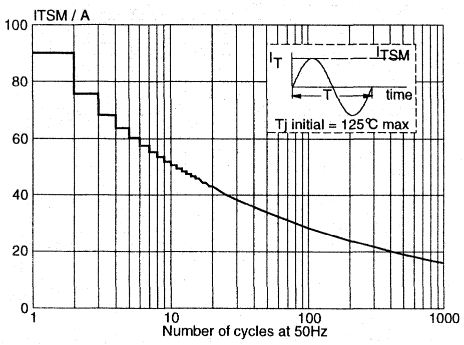


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

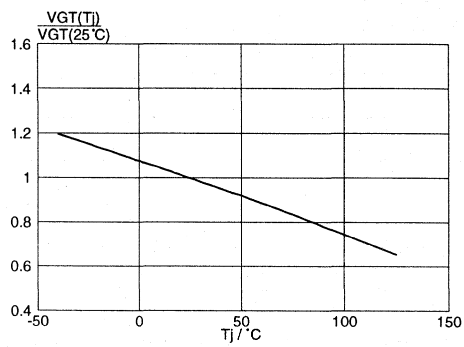


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25^{\circ}C)$, versus junction temperature T_j.

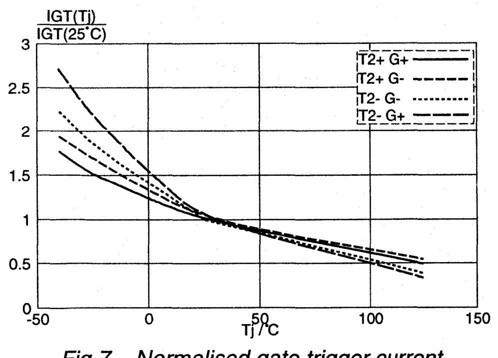


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

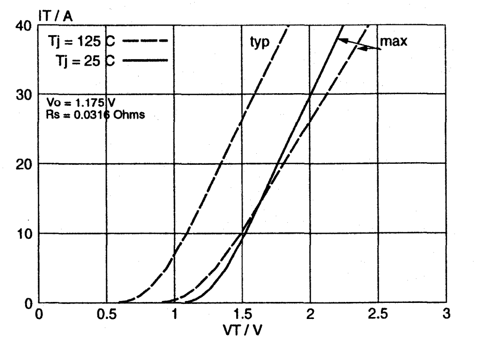


Fig.10. Typical and maximum on-state characteristic.

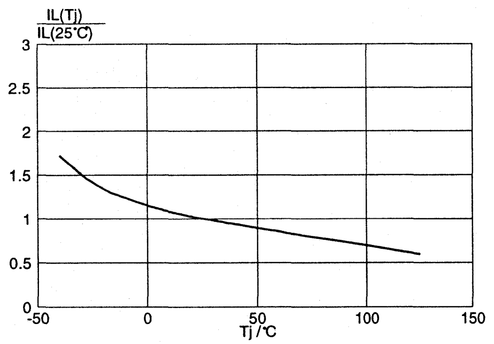


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.

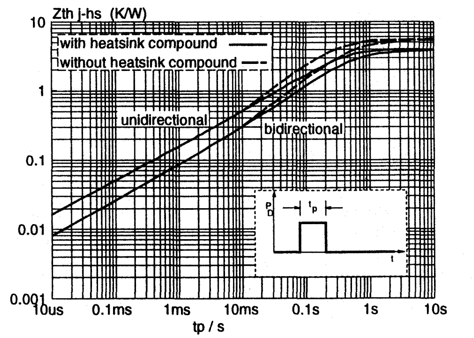


Fig.11. Transient thermal impedance $Z_{th\,j\text{-}hs}$, versus pulse width t_p.

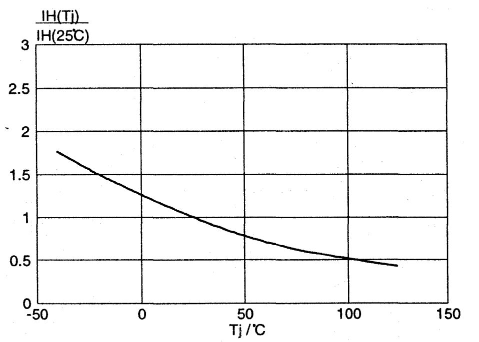


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j.

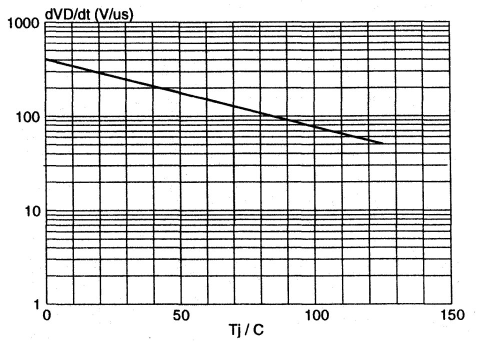


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

GENERAL DESCRIPTION

Glass passivated triacs in a plastic envelope, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

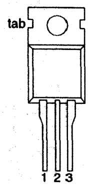
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT139-	**500**	**600**	**800**	
	BT139-	**500F**	**600F**	**800F**	
	BT139-	**500G**	**600G**	**800G**	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	16	16	16	A
I_{TSM}	Non-repetitive peak on-state current	140	140	140	A

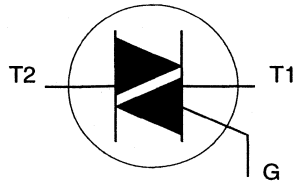
PINNING - TO220AB

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
tab	main terminal 2

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	**-600**	**-800**	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 99$ ˚C	-	16			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 20 ms	-	140			A
		t = 16.7 ms	-	150			A
I^2t	I^2t for fusing	t = 10 ms	-	98			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs					
		T2+ G+	-	50			A/µs
		T2+ G-	-	50			A/µs
		T2- G-	-	50			A/µs
		T2- G+	-	10			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base	full cycle	-	-	1.2	K/W
		half cycle	-	-	1.7	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.			UNIT
		BT139-			**...**	**...F**	**...G**	
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A						
		T2+ G+	-	5	35	25	50	mA
		T2+ G-	-	8	35	25	50	mA
		T2- G-	-	10	35	25	50	mA
		T2- G+	-	22	70	70	100	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A						
		T2+ G+	-	7	40	40	60	mA
		T2+ G-	-	20	60	60	90	mA
		T2- G-	-	8	40	40	60	mA
		T2- G+	-	10	60	60	90	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	6	30	30	60	mA
V_T	On-state voltage	I_T = 20 A	-	1.2	1.6			V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5			V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-			V
I_D	Off-state leakage current	$V_D = V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5			mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.			TYP.	MAX.	UNIT
		BT139-	**...**	**...F**	**...G**			
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	100	50	200	250	-	V/µs
dV_{com}/dt	Critical rate of change of commutating voltage	V_{DM} = 400 V; T_j = 95 ˚C; $I_{T(RMS)}$ = 16 A; dI_{com}/dt = 7.2 A/ms; gate open circuit	-	-	10	20	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 20 A; $V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	-	-	2	-	µs

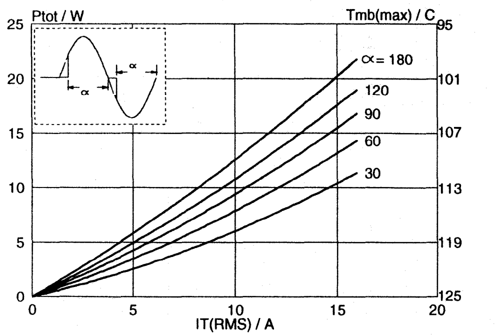


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

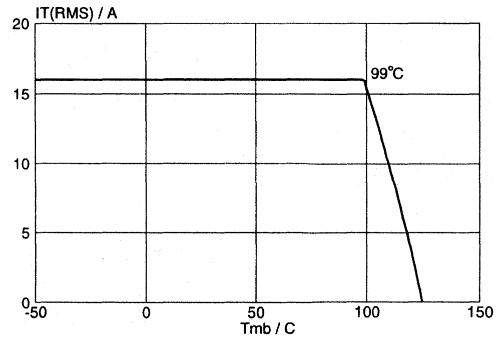


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

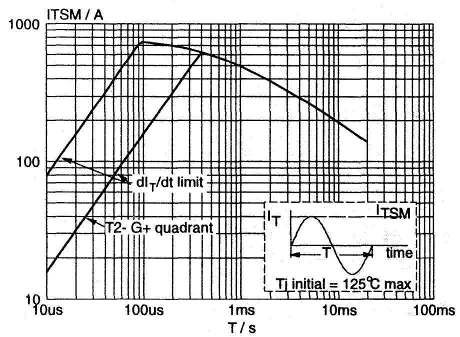


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

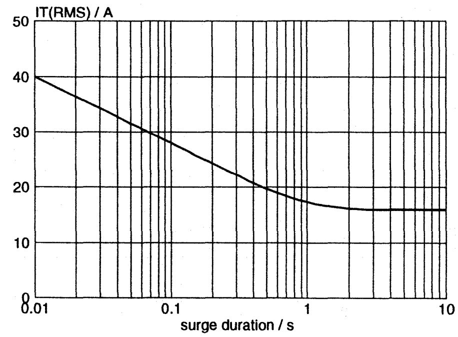


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 99^{\circ}C$.

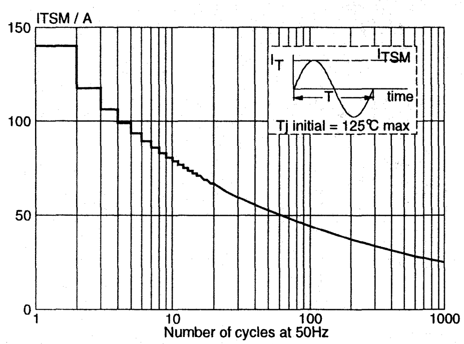


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

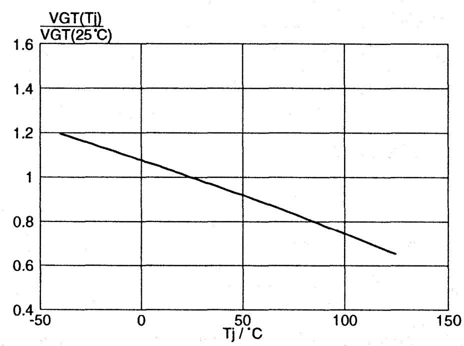


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25^{\circ}C)$, versus junction temperature T_j.

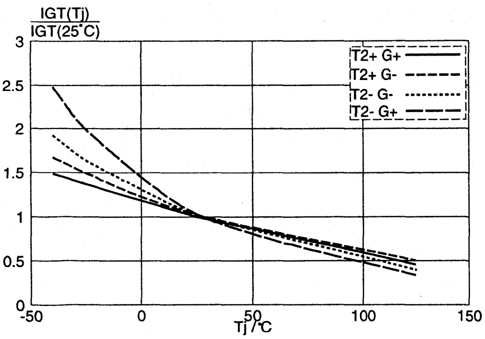


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature T_j.

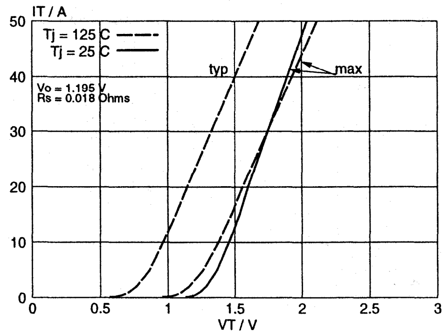


Fig.10. Typical and maximum on-state characteristic.

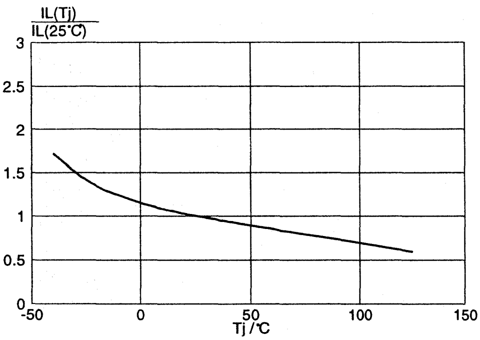


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature T_j.

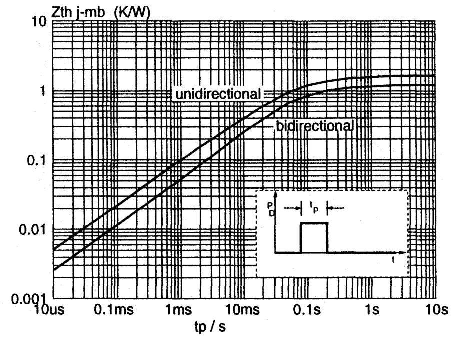


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width t_p.

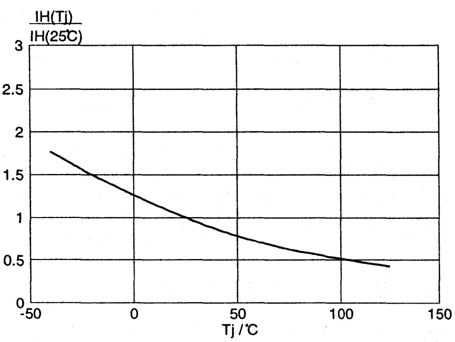


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature T_j.

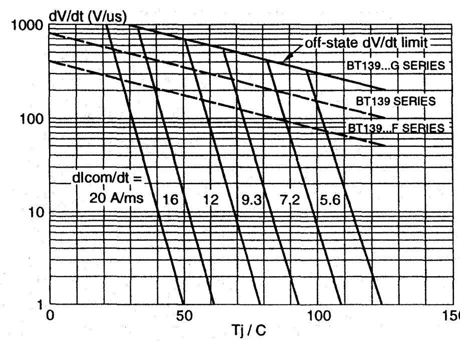


Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation dI_T/dt. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation dI_T/dt.

Triacs sensitive gate

BT139 series E

GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

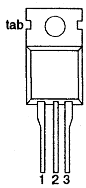
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT139-	500E	600E	800E	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	16	16	16	A
I_{TSM}	Non-repetitive peak on-state current	140	140	140	A

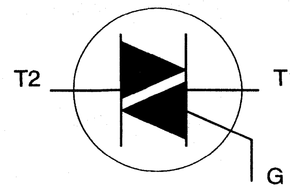
PINNING - TO220AB

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
tab	main terminal 2

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	-600	-800	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 99$ ˚C	-	16			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 20 ms	-	140			A
		t = 16.7 ms	-	150			A
I^2t	I^2t for fusing	t = 10 ms	-	98			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs					
		T2+ G+	-	50			A/µs
		T2+ G-	-	50			A/µs
		T2- G-	-	50			A/µs
		T2- G+	-	10			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	full cycle	-	-	1.2	K/W
		half cycle	-	-	1.7	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	-	2.5	10	mA
		T2+ G-	-	4.0	10	mA
		T2- G-	-	5.0	10	mA
		T2- G+	-	11	25	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	3.2	30	mA
		T2+ G-	-	16	40	mA
		T2- G-	-	4.0	30	mA
		T2- G+	-	5.5	40	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	4.0	30	mA
V_T	On-state voltage	I_T = 20 A	-	1.2	1.6	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	-	50	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 20 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs

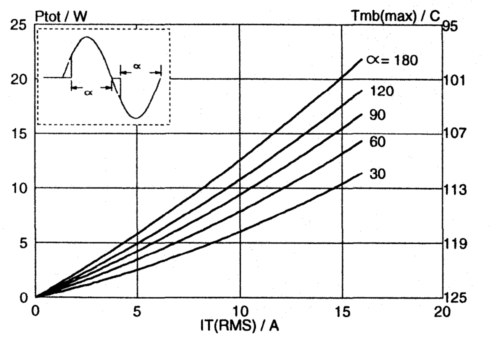


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

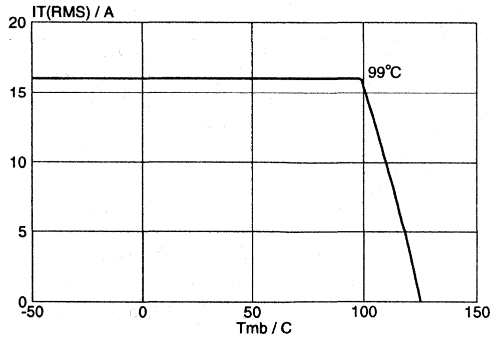


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

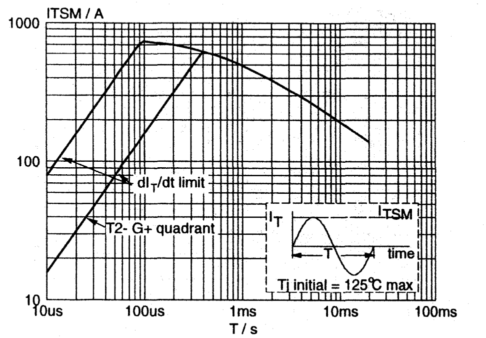


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

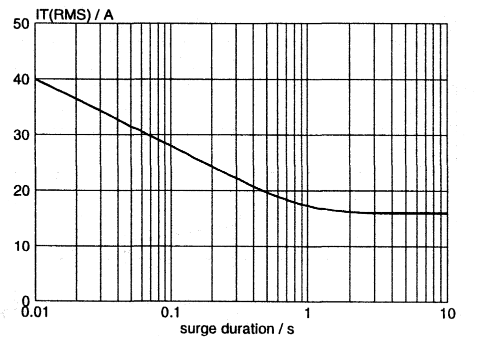


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 99$˚C.

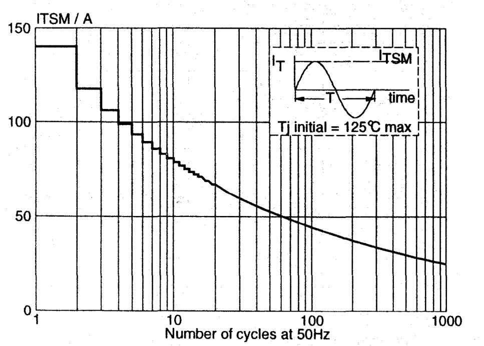


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

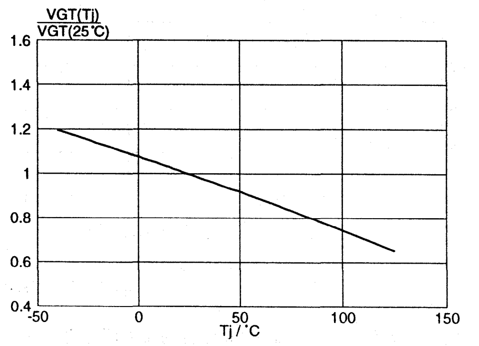


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25˚C)$, versus junction temperature T_j.

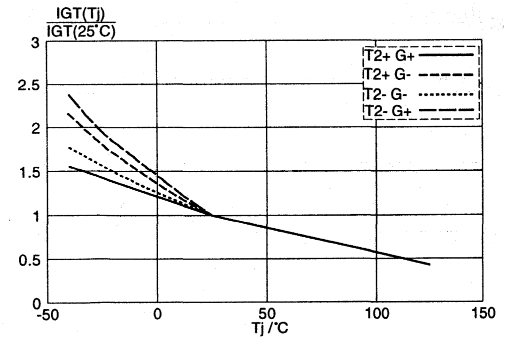


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/I_{GT}(25˚C)$, versus junction temperature T_j.

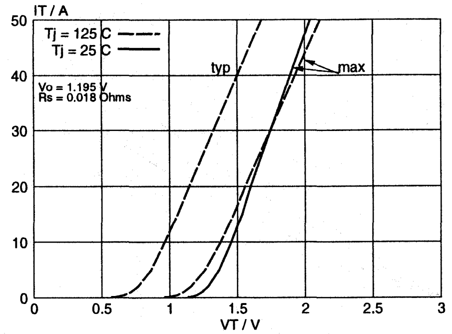


Fig.10. Typical and maximum on-state characteristic.

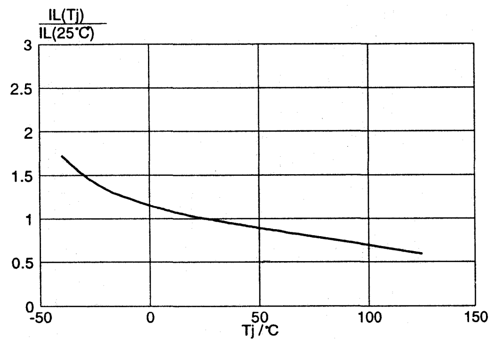


Fig.8. Normalised latching current $I_L(T_j)/I_L(25˚C)$, versus junction temperature T_j.

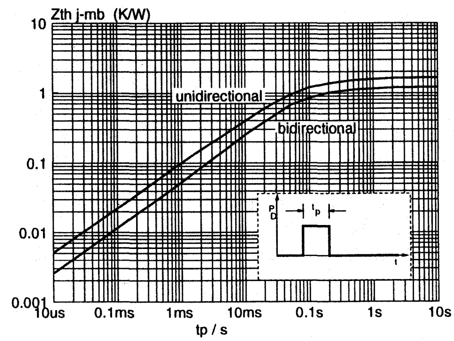


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width t_p.

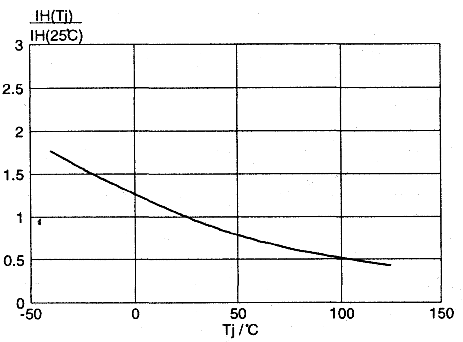


Fig.9. Normalised holding current $I_H(T_j)/I_H(25˚C)$, versus junction temperature T_j.

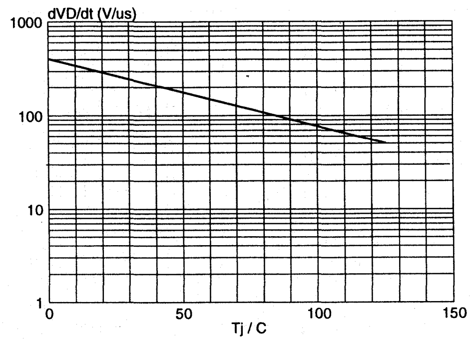


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

Triacs high noise immunity

BT139 series H

GENERAL DESCRIPTION

Glass passivated triacs in a plastic envelope, intended for use in applications requiring high noise immunity in addition to high, bidirectional blocking voltage capability and thermal cycling performance. Typical applications include motor control, industrial lighting, heating and static switching.

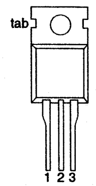
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT139-	500H	600H	800H	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	16	16	16	A
I_{TSM}	Non-repetitive peak on-state current	140	140	140	A

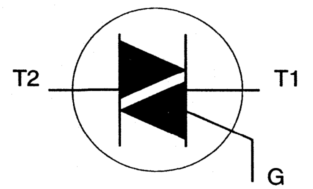
PINNING - TO220AB

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
tab	main terminal 2

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	-600	-800	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 99$ ˚C	-	16			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 20 ms	-	140			A
		t = 16.7 ms	-	150			A
I^2t	I^2t for fusing	t = 10 ms	-	98			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs					
		T2+ G+	-	50			A/µs
		T2+ G-	-	50			A/µs
		T2- G-	-	50			A/µs
		T2- G+	-	10			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	full cycle	-	-	1.2	K/W
		half cycle	-	-	1.7	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	10	14	50	mA
		T2+ G-	10	17	50	mA
		T2- G-	10	18	50	mA
		T2- G+	10	40	100	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	10	60	mA
		T2+ G-	-	25	90	mA
		T2- G-	-	12	60	mA
		T2- G+	-	14	90	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	8	60	mA
V_T	On-state voltage	I_T = 20 A	-	1.2	1.6	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	$V_D = V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	200	500	-	V/μs
dV_{com}/dt	Critical rate of change of commutating voltage	V_{DM} = 400 V; T_j = 95 ˚C; $I_{T(RMS)}$ = 16 A; dI_{com}/dt = 7.2 A/ms; gate open circuit	10	20	-	V/μs
t_{gt}	Gate controlled turn-on time	I_{TM} = 20 A; $V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/μs	-	2	-	μs

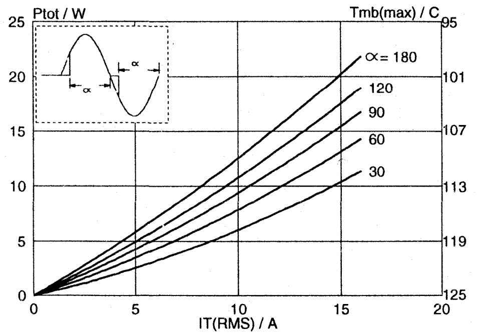


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

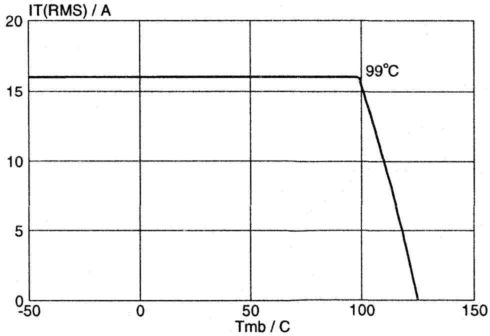


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

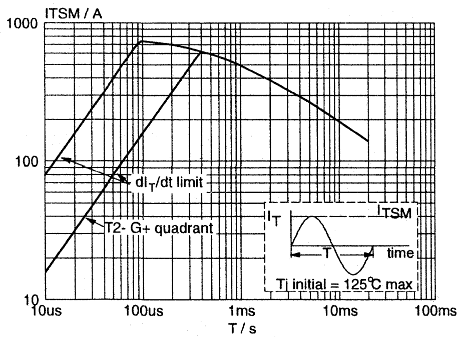


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

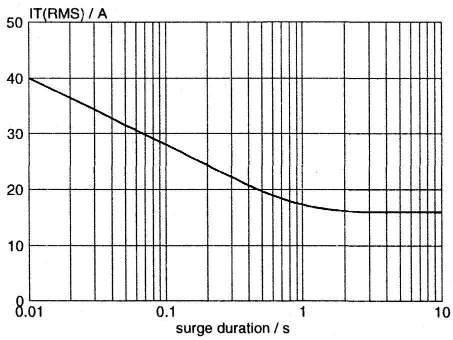


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 99$˚C.

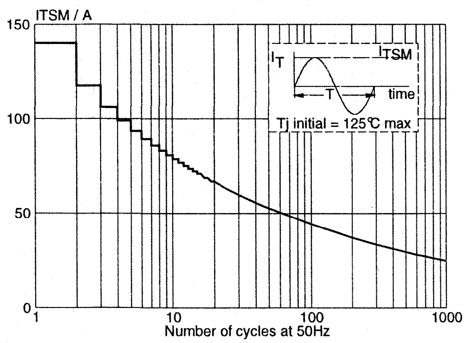


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

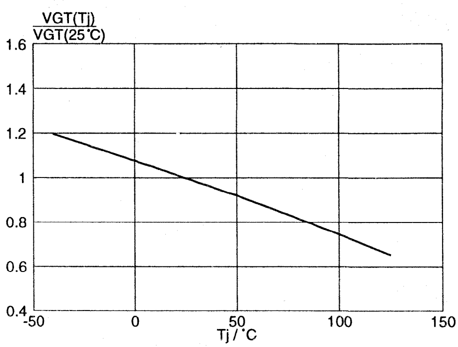


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25˚C)$, versus junction temperature T_j.

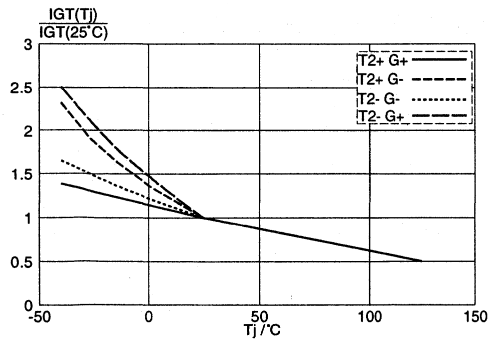


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

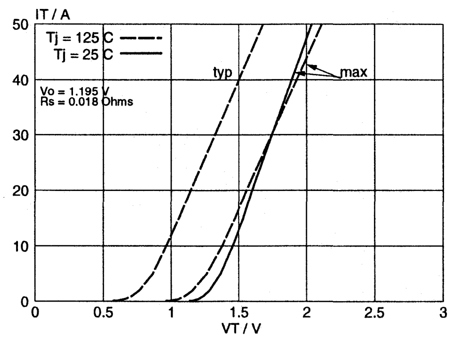


Fig.10. Typical and maximum on-state characteristic.

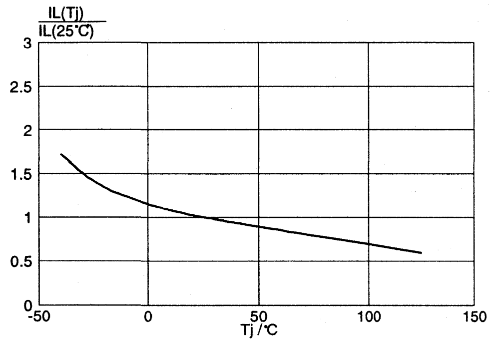


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.

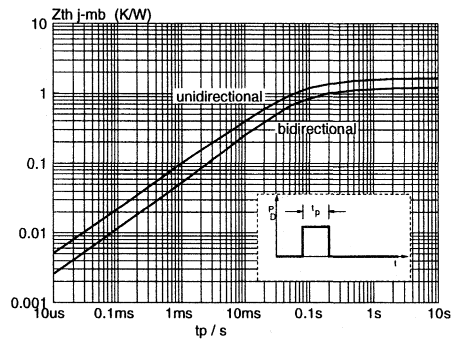


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width t_p.

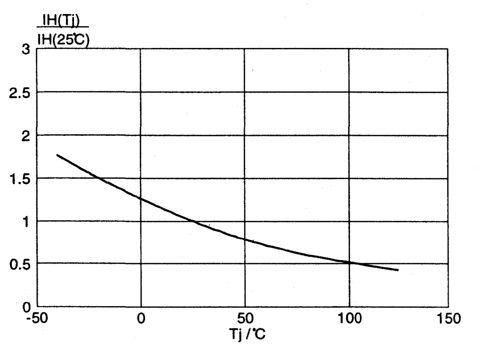


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j.

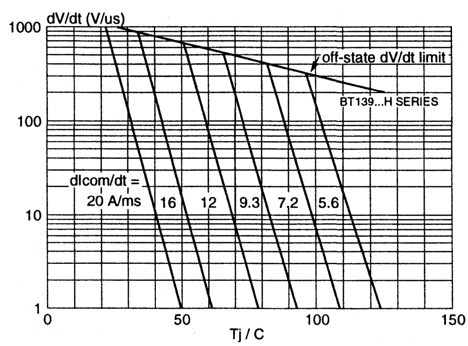


Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation dI_T/dt. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation dI_T/dt.

GENERAL DESCRIPTION

Glass passivated triacs in a full pack, plastic envelope, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

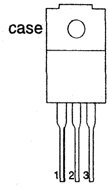
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT139F-	**500**	**600**	**800**	
	BT139F-	**500F**	**600F**	**800F**	
	BT139F-	**500G**	**600G**	**800G**	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	16	16	16	A
I_{TSM}	Non-repetitive peak on-state current	140	140	140	A

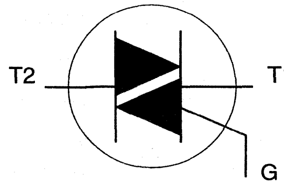
PINNING - SOT186

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	**-600**	**-800**	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{hs} \leq 38$ ˚C	-	16			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 20 ms	-	140			A
		t = 16.7 ms	-	150			A
I^2t	I^2t for fusing	t = 10 ms	-	98			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	I_{TM} = 20 A; I_G = 0.2 A; dI_G/dt = 0.2 A/µs					
		T2+ G+	-	50			A/µs
		T2+ G-	-	50			A/µs
		T2- G-	-	50			A/µs
		T2- G+	-	10			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-hs}$	Thermal resistance junction to heatsink	full or half cycle				
		with heatsink compound	-	-	4.0	K/W
		without heatsink compound	-	-	5.5	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	in free air	-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.			UNIT
		BT139F-			...	...F	...G	
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A						
		T2+ G+	-	5	35	25	50	mA
		T2+ G-	-	8	35	25	50	mA
		T2- G-	-	10	35	25	50	mA
		T2- G+	-	22	70	70	100	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A						
		T2+ G+	-	7	40	40	60	mA
		T2+ G-	-	20	60	60	90	mA
		T2- G-	-	8	40	40	60	mA
		T2- G+	-	10	60	60	90	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	6	30	30	60	mA
V_T	On-state voltage	I_T = 20 A	-	1.2	1.6			V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5			V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-			V
I_D	Off-state leakage current	$V_D = V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5			mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.			TYP.	MAX.	UNIT
		BT139F-	...	...F	...G			
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	100	50	200	250	-	V/µs
dV_{com}/dt	Critical rate of change of commutating voltage	V_{DM} = 400 V; T_j = 95 ˚C; $I_{T(RMS)}$ = 16 A; dI_{com}/dt = 7.2 A/ms; gate open circuit	-	-	10	20	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 20 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	-	-	2	-	µs

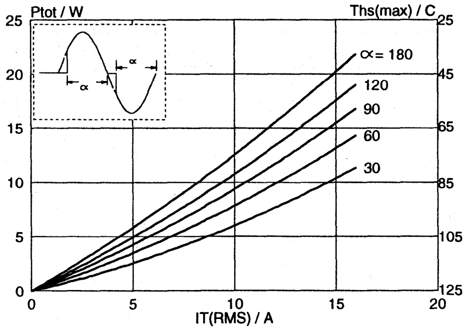


Fig. 1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

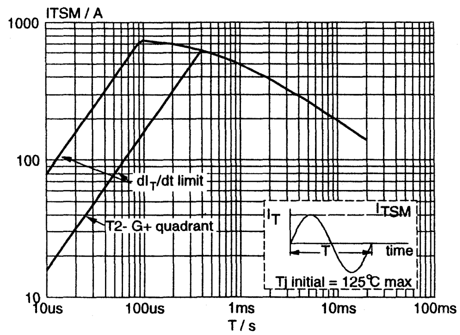


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq$ 20ms.

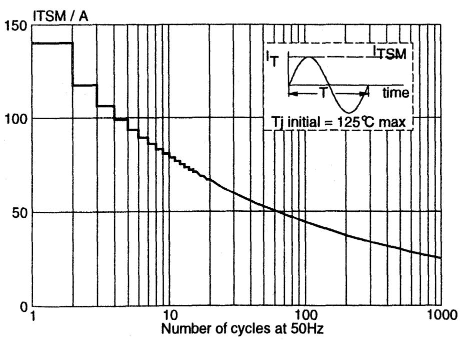


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

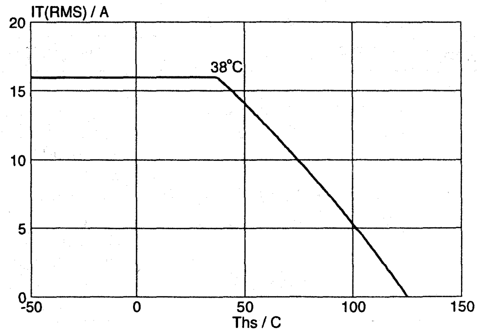


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature T_{hs}.

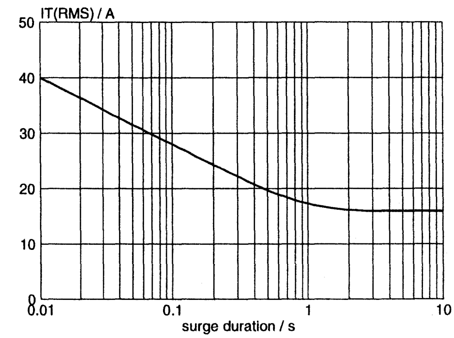


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq$ 38˚C.

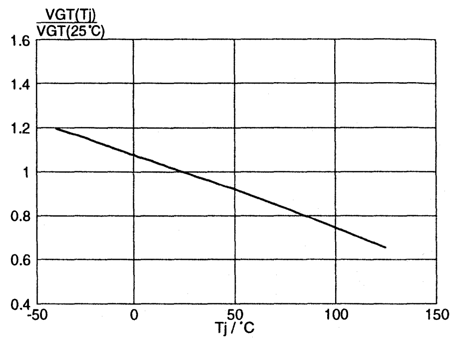


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25˚C)$, versus junction temperature T_j.

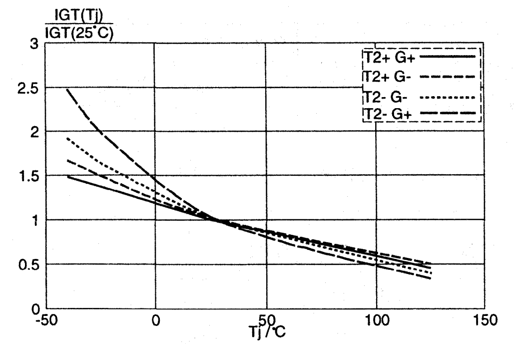


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/I_{GT}(25˚C)$, versus junction temperature T_j.

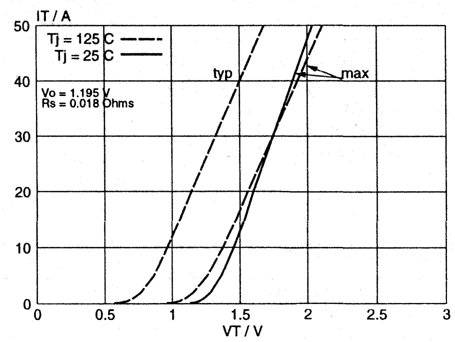


Fig.10. Typical and maximum on-state characteristic.

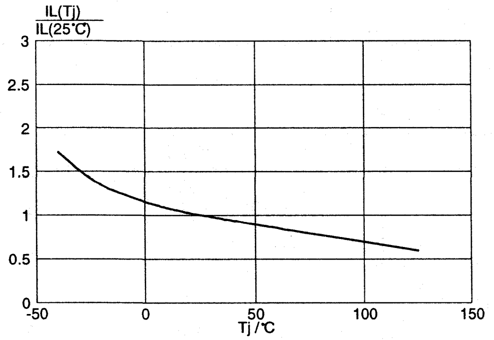


Fig.8. Normalised latching current $I_L(T_j)/I_L(25˚C)$, versus junction temperature T_j.

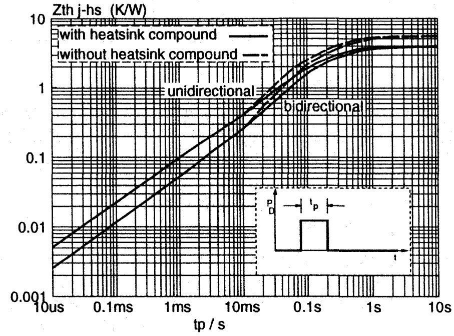


Fig.11. Transient thermal impedance $Z_{th\,j\text{-}hs}$, versus pulse width t_p.

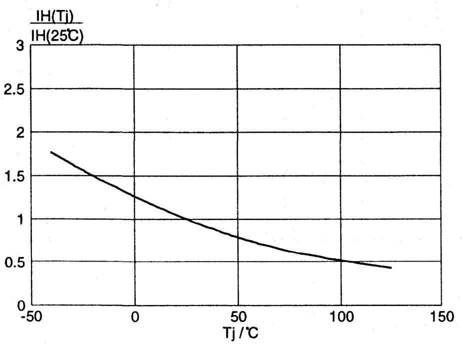


Fig.9. Normalised holding current $I_H(T_j)/I_H(25˚C)$, versus junction temperature T_j.

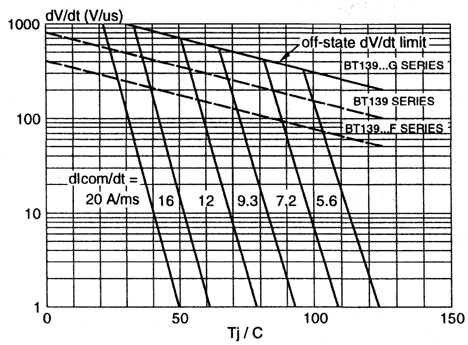


Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation dI_T/dt. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation dI_T/dt.

GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a full pack plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

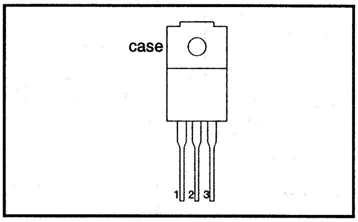
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT139F-	500E	600E	800E	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	16	16	16	A
I_{TSM}	Non-repetitive peak on-state current	140	140	140	A

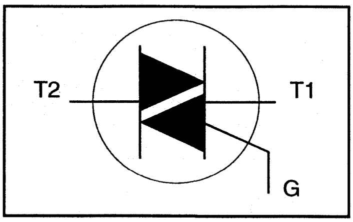
PINNING - SOT186

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	-600	-800	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{hs} \leq 38$ ˚C	-	16			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 20 ms	-	140			A
		t = 16.7 ms	-	150			A
I^2t	I^2t for fusing	t = 10 ms	-	98			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs					
		T2+ G+	-	50			A/µs
		T2+ G-	-	50			A/µs
		T2- G-	-	50			A/µs
		T2- G+	-	10			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	full or half cycle				
		with heatsink compound	-	-	4.0	K/W
		without heatsink compound	-	-	5.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	-	2.5	10	mA
		T2+ G-	-	4.0	10	mA
		T2- G-	-	5.0	10	mA
		T2- G+	-	11	25	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	3.2	30	mA
		T2+ G-	-	16	40	mA
		T2- G-	-	4.0	30	mA
		T2- G+	-	5.5	40	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	4.0	30	mA
V_T	On-state voltage	I_T = 20 A	-	1.2	1.6	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	-	50	-	V/μs
t_{gt}	Gate controlled turn-on time	V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/μs; I_{TM} = 20 A	-	2	-	μs

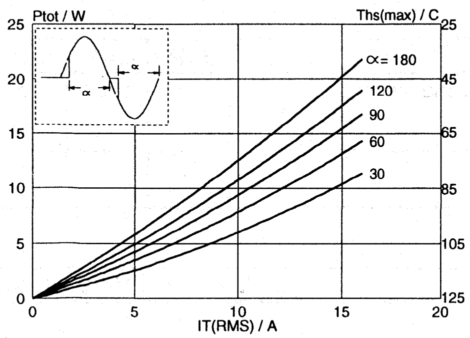


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

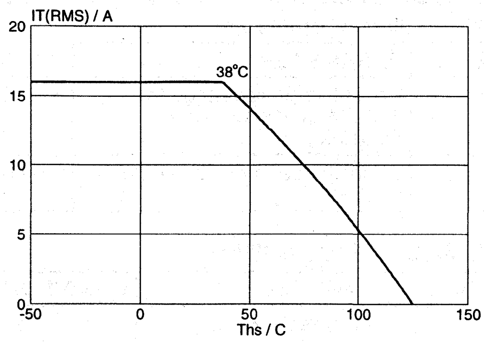


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature T_{hs}.

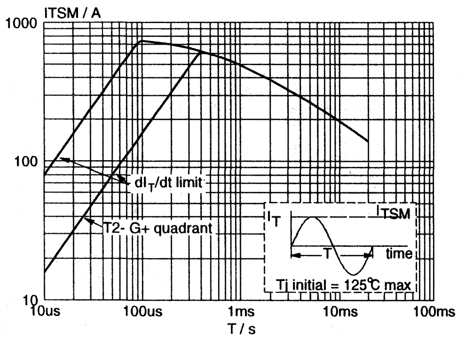


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

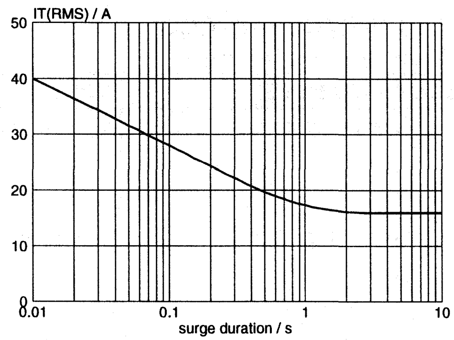


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 38$°C.

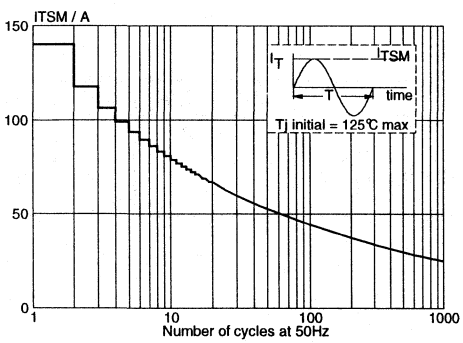


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

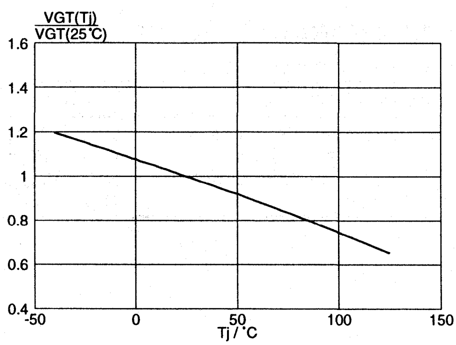


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25$°C$)$, versus junction temperature T_j.

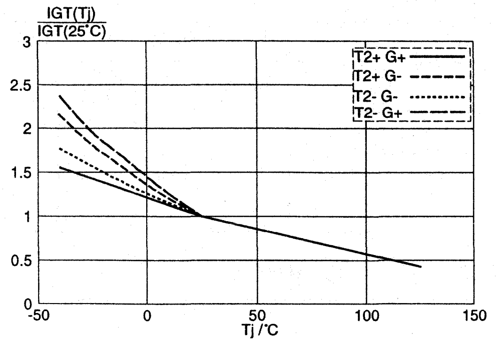


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/\ I_{GT}(25˚C)$, versus junction temperature T_j.

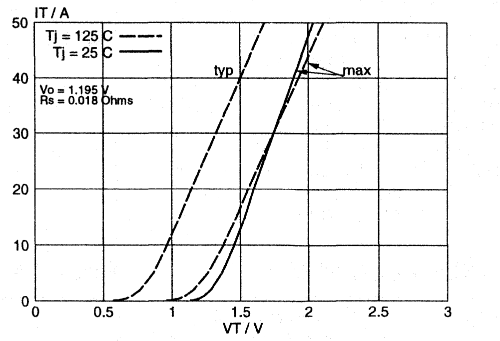


Fig.10. Typical and maximum on-state characteristic.

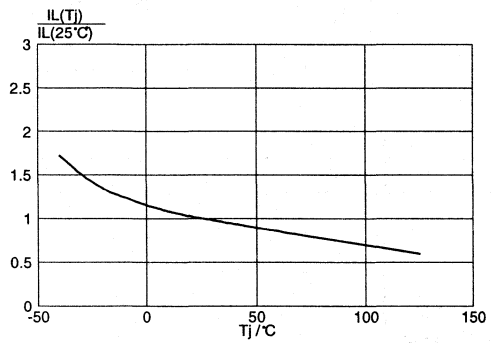


Fig.8. Normalised latching current $I_L(T_j)/\ I_L(25˚C)$, versus junction temperature T_j.

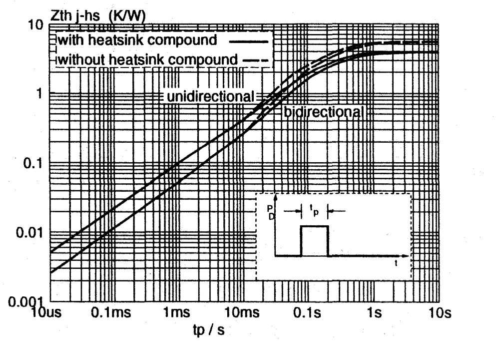


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}hs}$, versus pulse width t_p.

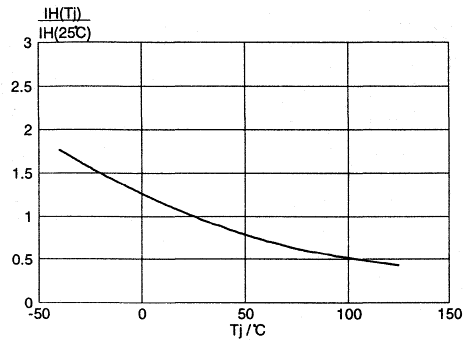


Fig.9. Normalised holding current $I_H(T_j)/\ I_H(25˚C)$, versus junction temperature T_j.

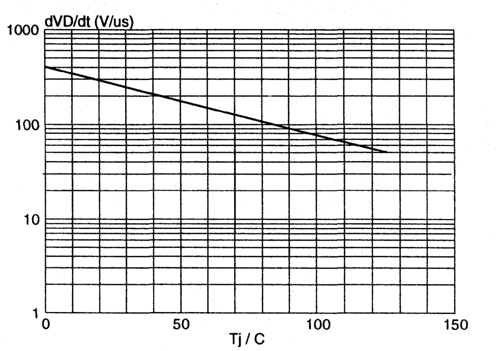


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

Triacs high noise immunity | BT139F series H

GENERAL DESCRIPTION

Glass passivated triacs in a full pack, plastic envelope, intended for use in applications requiring high noise immunity in addition to high, bidirectional blocking voltage capability and thermal cycling performance. Typical applications include motor control, industrial lighting, heating and static switching.

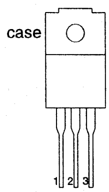
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT139F-	500H	600H	800H	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	16	16	16	A
I_{TSM}	Non-repetitive peak on-state current	140	140	140	A

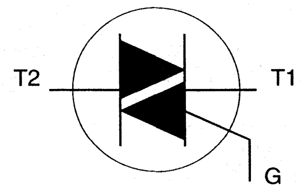
PINNING - SOT186

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	-600	-800	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{hs} \leq 38$ ˚C	-		16		A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 20 ms	-		140		A
		t = 16.7 ms	-		150		A
I^2t	I^2t for fusing	t = 10 ms	-		98		A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs					
		T2+ G+	-		50		A/µs
		T2+ G-	-		50		A/µs
		T2- G-	-		50		A/µs
		T2- G+	-		10		A/µs
I_{GM}	Peak gate current		-		2		A
V_{GM}	Peak gate voltage		-		5		V
P_{GM}	Peak gate power		-		5		W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-		0.5		W
T_{stg}	Storage temperature		-40		150		˚C
T_j	Operating junction temperature		-		125		˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	full or half cycle				
		with heatsink compound	-	-	4.0	K/W
		without heatsink compound	-	-	5.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	10	14	50	mA
		T2+ G-	10	17	50	mA
		T2- G-	10	18	50	mA
		T2- G+	10	40	100	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	10	60	mA
		T2+ G-	-	25	90	mA
		T2- G-	-	12	60	mA
		T2- G+	-	14	90	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	8	60	mA
V_T	On-state voltage	I_T = 20 A	-	1.2	1.6	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	200	500	-	V/µs
dV_{com}/dt	Critical rate of change of commutating voltage	V_{DM} = 400 V; T_j = 95 ˚C; $I_{T(RMS)}$ = 16 A; dI_{com}/dt = 7.2 A/ms; gate open circuit	10	20	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 20 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs

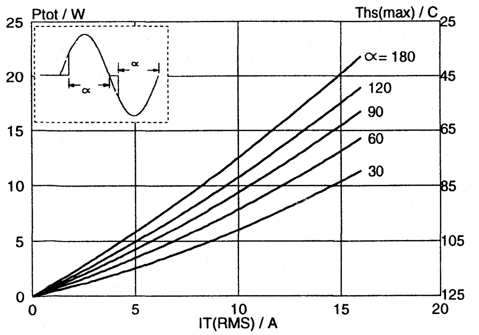


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

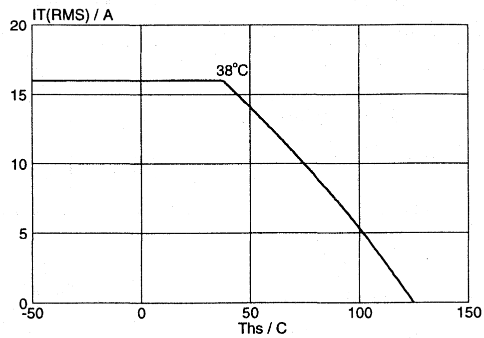


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature T_{hs}.

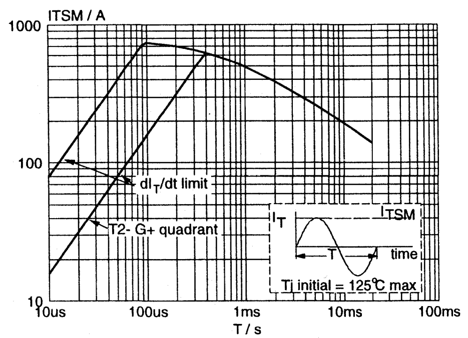


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq$ 20ms.

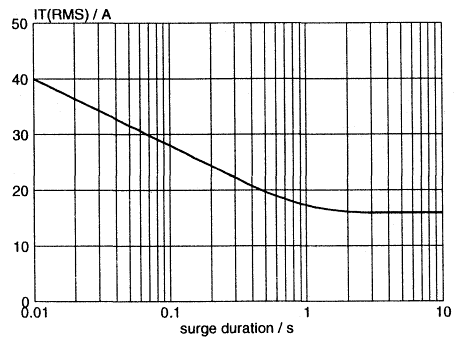


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq$ 38˚C.

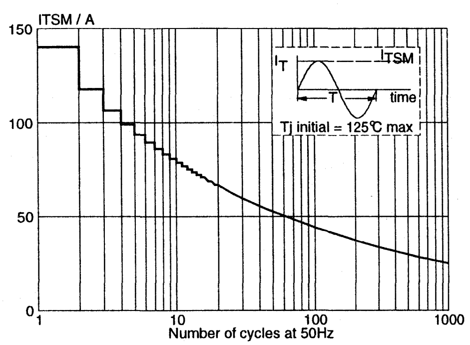


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

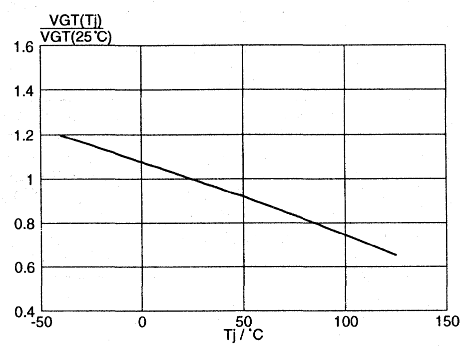


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)$/ V_{GT}(25˚C), versus junction temperature T_j.

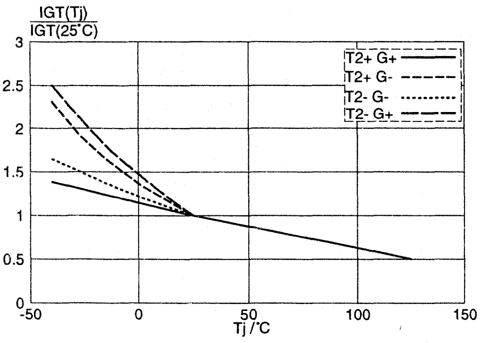


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/\ I_{GT}(25˚C)$, versus junction temperature T_j.

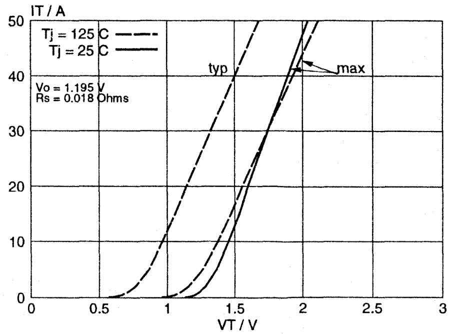


Fig.10. Typical and maximum on-state characteristic.

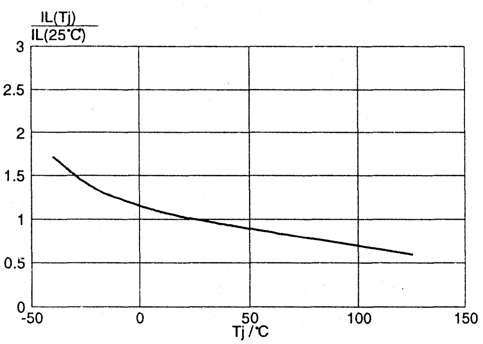


Fig.8. Normalised latching current $I_L(T_j)/\ I_L(25˚C)$, versus junction temperature T_j.

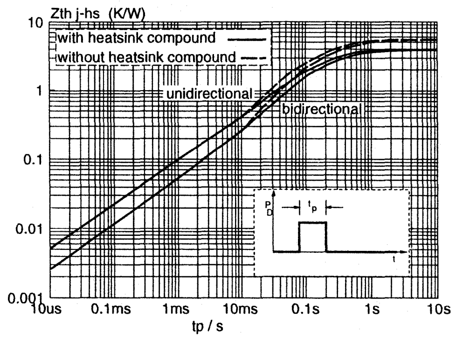


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}hs}$, versus pulse width t_p.

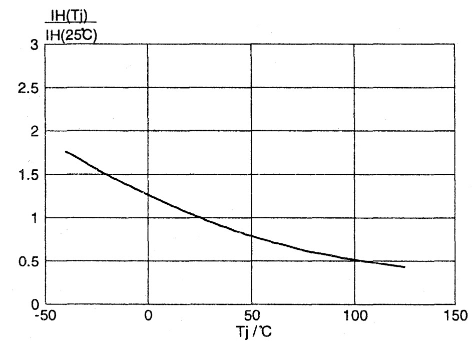


Fig.9. Normalised holding current $I_H(T_j)/\ I_H(25˚C)$, versus junction temperature T_j.

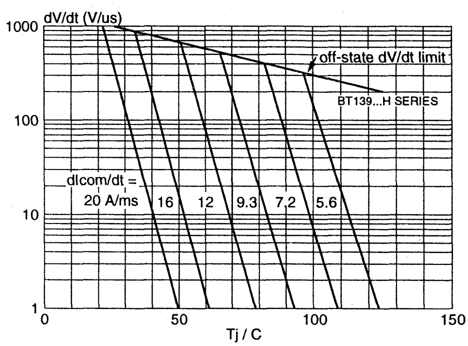


Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation dI_T/dt. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation dI_T/dt.

GENERAL DESCRIPTION

Glass passivated triacs in a full pack, plastic envelope, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

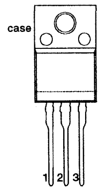
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT139X-	500	600	800	
	BT139X-	500F	600F	800F	
	BT139X-	500G	600G	800G	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	16	16	16	A
I_{TSM}	Non-repetitive peak on-state current	140	140	140	A

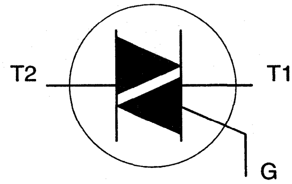
PINNING - SOT186A

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	-600	-800	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{hs} \leq 38$ ˚C	-	16			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 20 ms	-	140			A
		t = 16.7 ms	-	150			A
I^2t	I^2t for fusing	t = 10 ms	-	98			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs					
		T2+ G+	-	50			A/µs
		T2+ G-	-	50			A/µs
		T2- G-	-	50			A/µs
		T2- G+	-	10			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	full or half cycle				
		with heatsink compound	-	-	4.0	K/W
		without heatsink compound	-	-	5.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.			UNIT
		BT139X-			...	...F	...G	
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A						
		T2+ G+	-	5	35	25	50	mA
		T2+ G-	-	8	35	25	50	mA
		T2- G-	-	10	35	25	50	mA
		T2- G+	-	22	70	70	100	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A						
		T2+ G+	-	7	40	40	60	mA
		T2+ G-	-	20	60	60	90	mA
		T2- G-	-	8	40	40	60	mA
		T2- G+	-	10	60	60	90	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	6	30	30	60	mA
V_T	On-state voltage	I_T = 20 A	-	1.2	1.6			V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5			V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-			V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5			mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.			TYP.	MAX.	UNIT
		BT139X-	**...**	**...F**	**...G**			
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	100	50	200	250	-	V/µs
dV_{com}/dt	Critical rate of change of commutating voltage	V_{DM} = 400 V; T_j = 95 ˚C; $I_{T(RMS)}$ = 16 A; dI_{com}/dt = 7.2 A/ms; gate open circuit	-	-	10	20	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 20 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	-	-	2	-	µs

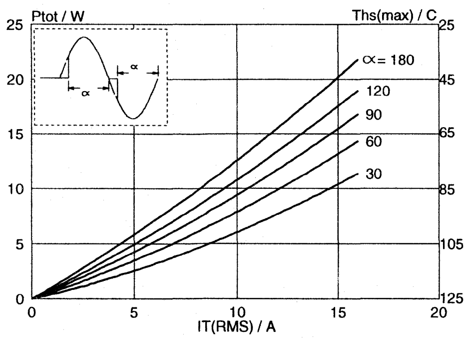


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

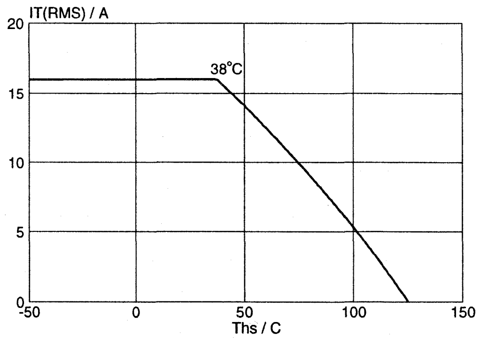


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature T_{hs}.

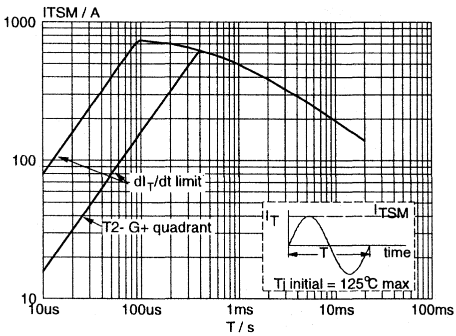


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

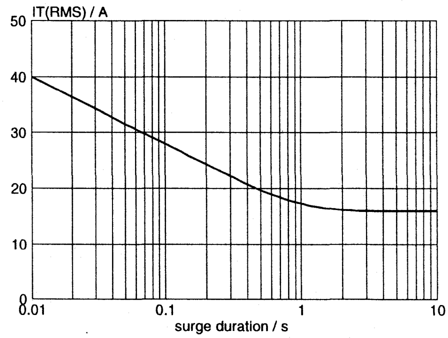


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 38^{\circ}C$.

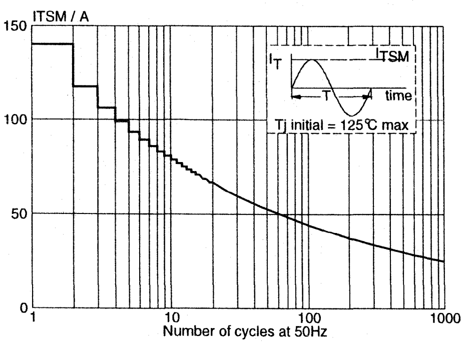


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

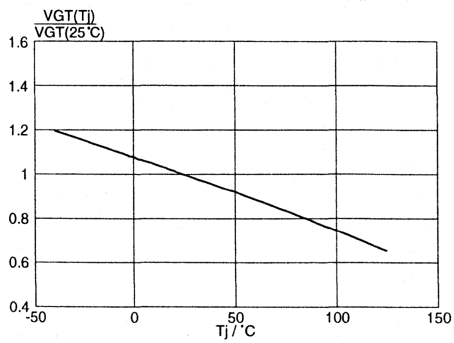


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25^{\circ}C)$, versus junction temperature T_j.

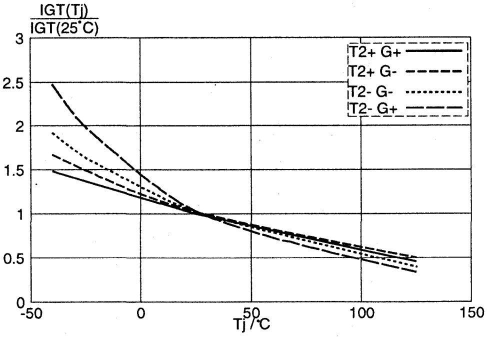


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/\ I_{GT}(25^\circ C)$, versus junction temperature T_j.

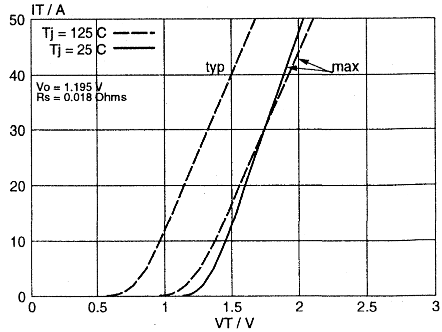


Fig.10. Typical and maximum on-state characteristic.

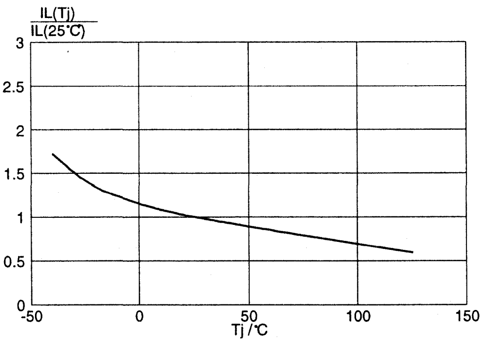


Fig.8. Normalised latching current $I_L(T_j)/\ I_L(25^\circ C)$, versus junction temperature T_j.

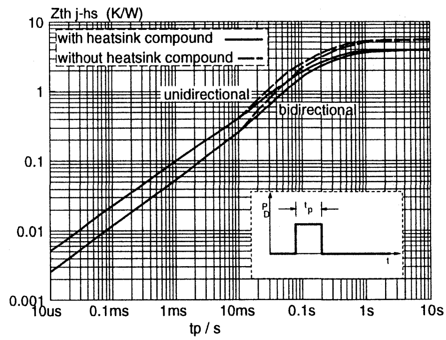


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}hs}$, versus pulse width t_p.

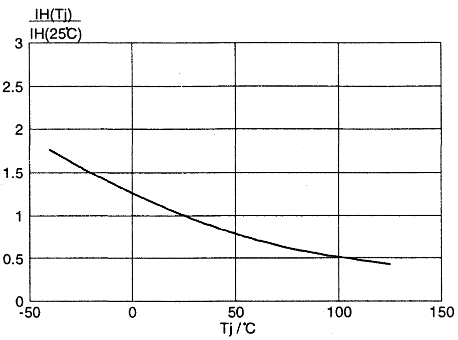


Fig.9. Normalised holding current $I_H(T_j)/\ I_H(25^\circ C)$, versus junction temperature T_j.

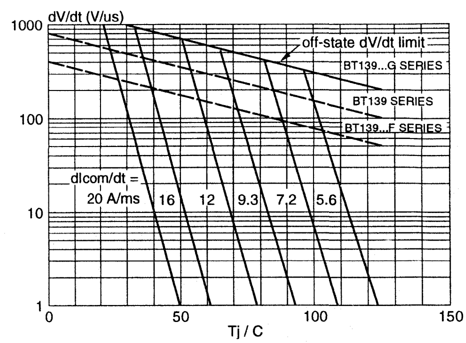


Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation dI_T/dt. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation dI_T/dt.

Triacs sensitive gate

BT139X series E

GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a full pack plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

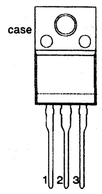
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT139X-	500E	600E	800E	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	16	16	16	A
I_{TSM}	Non-repetitive peak on-state current	140	140	140	A

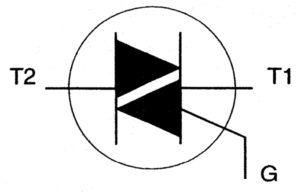
PINNING - SOT186A

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	-600	-800	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{hs} \leq 38$ ˚C	-	16			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 20 ms	-	140			A
		t = 16.7 ms	-	150			A
I^2t	I^2t for fusing	t = 10 ms	-	98			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs					
		T2+ G+	-	50			A/µs
		T2+ G-	-	50			A/µs
		T2- G-	-	50			A/µs
		T2- G+	-	10			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-hs}$	Thermal resistance junction to heatsink	full or half cycle with heatsink compound	-	-	4.0	K/W
		without heatsink compound	-	-	5.5	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	in free air	-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	-	2.5	10	mA
		T2+ G-	-	4.0	10	mA
		T2- G-	-	5.0	10	mA
		T2- G+	-	11	25	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	3.2	30	mA
		T2+ G-	-	16	40	mA
		T2- G-	-	4.0	30	mA
		T2- G+	-	5.5	40	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	4.0	30	mA
V_T	On-state voltage	I_T = 20 A	-	1.2	1.6	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	$V_D = V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	-	50	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 20 A; $V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs

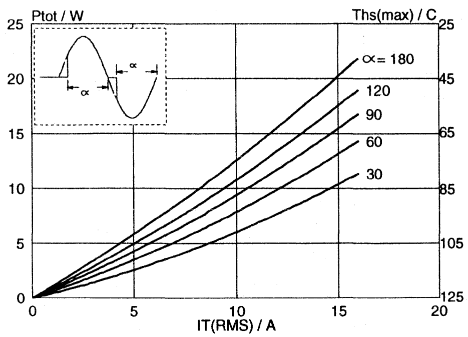


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

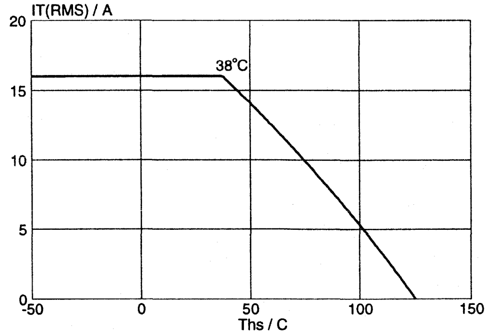


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature T_{hs}.

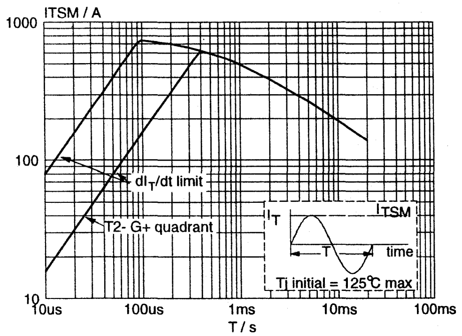


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

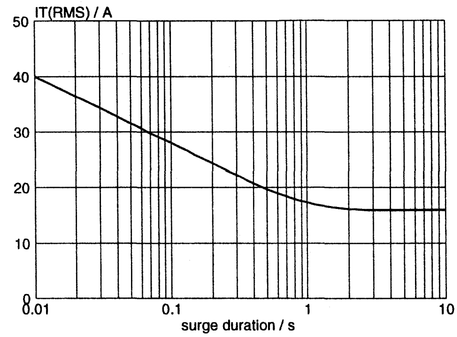


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 38$˚C.

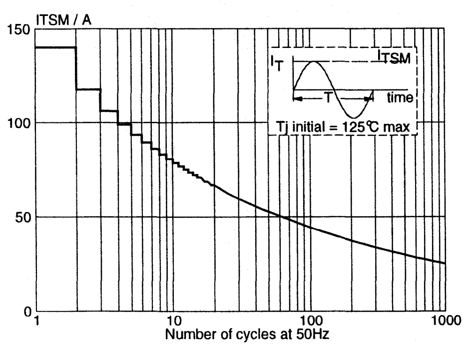


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

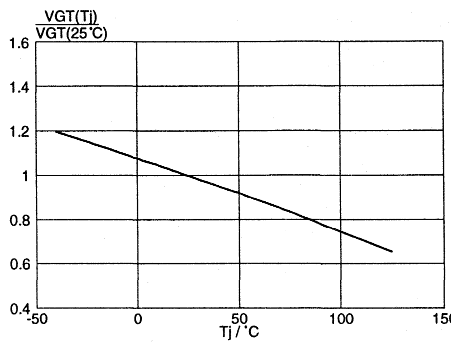


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25$˚C), versus junction temperature T_j.

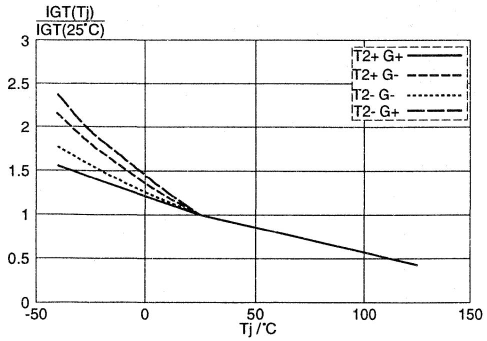


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

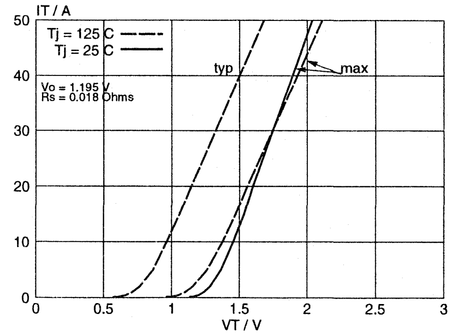


Fig.10. Typical and maximum on-state characteristic.

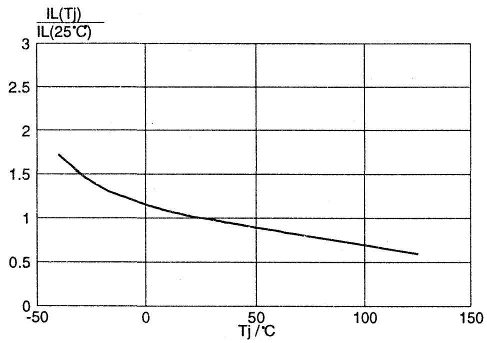


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.

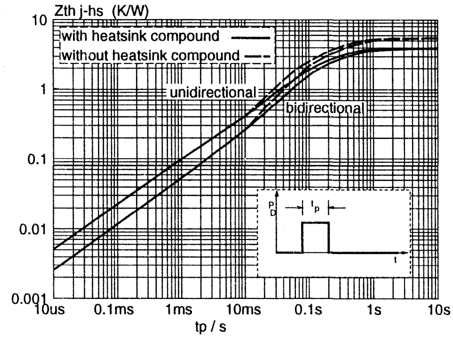


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}hs}$, versus pulse width t_p.

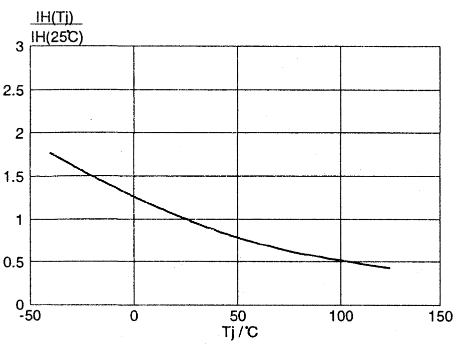


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j.

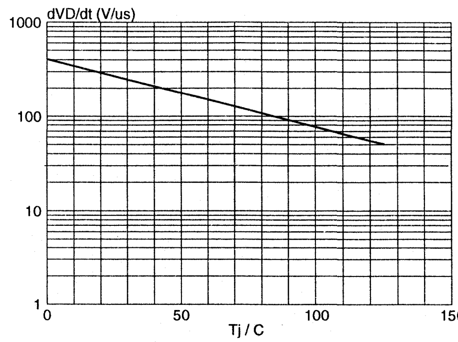


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

Triacs
high noise immunity

BT139X series H

GENERAL DESCRIPTION

Glass passivated triacs in a full pack, plastic envelope, intended for use in applications requiring high noise immunity in addition to high, bidirectional blocking voltage capability and thermal cycling performance. Typical applications include motor control, industrial lighting, heating and static switching.

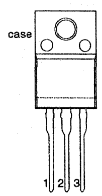
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT139X-	**500H**	**600H**	**800H**	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	16	16	16	A
I_{TSM}	Non-repetitive peak on-state current	140	140	140	A

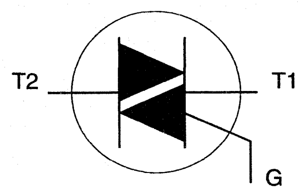
PINNING - SOT186A

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX. -500	MAX. -600	MAX. -800	UNIT
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{hs} \leq 38$ ˚C	-	16			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 20 ms	-	140			A
		t = 16.7 ms	-	150			A
I^2t	I^2t for fusing	t = 10 ms	-	98			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs					
		T2+ G+	-	50			A/µs
		T2+ G-	-	50			A/µs
		T2- G-	-	50			A/µs
		T2- G+	-	10			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	full or half cycle				
		with heatsink compound	-	-	4.0	K/W
		without heatsink compound	-	-	5.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	10	14	50	mA
		T2+ G-	10	17	50	mA
		T2- G-	10	18	50	mA
		T2- G+	10	40	100	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	10	60	mA
		T2+ G-	-	25	90	mA
		T2- G-	-	12	60	mA
		T2- G+	-	14	90	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	8	60	mA
V_T	On-state voltage	I_T = 20 A	-	1.2	1.6	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	$V_D = V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	200	500	-	V/µs
dV_{com}/dt	Critical rate of change of commutating voltage	V_{DM} = 400 V; T_j = 95 ˚C; $I_{T(RMS)}$ = 16 A; dI_{com}/dt = 7.2 A/ms; gate open circuit	10	20	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 20 A; $V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs

Triacs
high noise immunity

BT139X series H

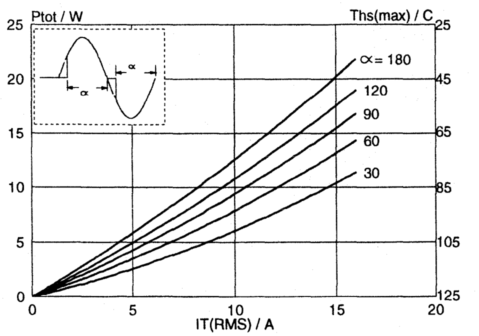


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

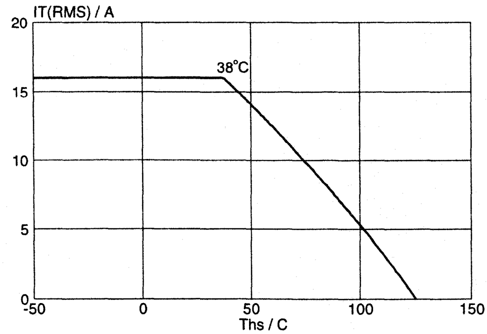


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature T_{hs}.

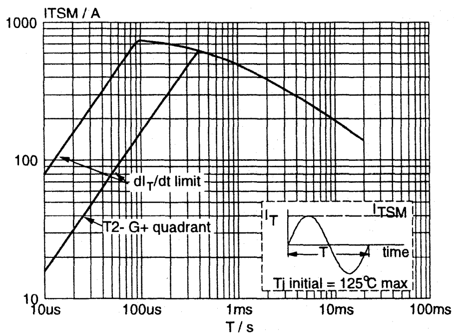


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq$ 20ms.

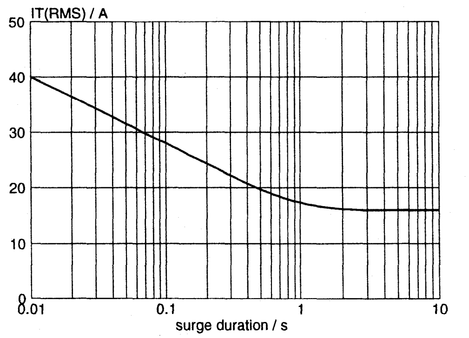


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq$ 38˚C.

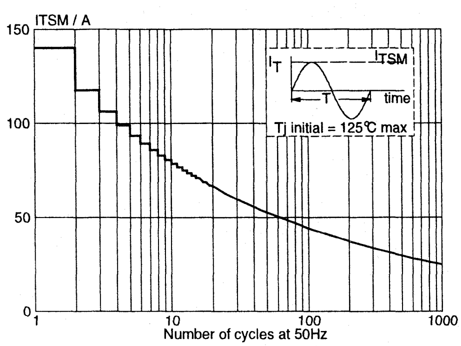


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

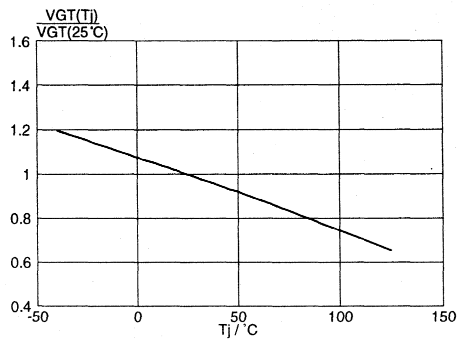


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)$/ V_{GT}(25˚C), versus junction temperature T_j.

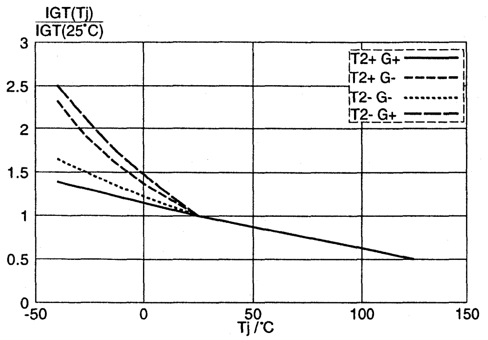


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

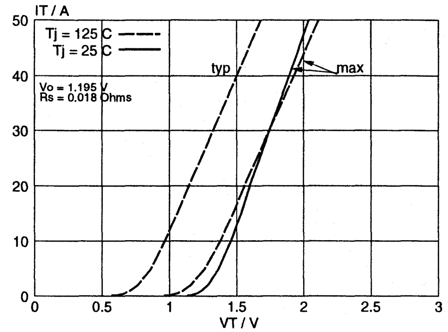


Fig.10. Typical and maximum on-state characteristic.

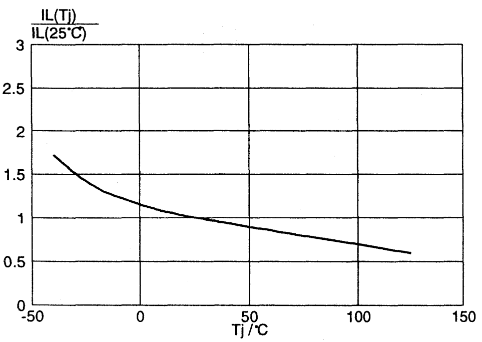


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.

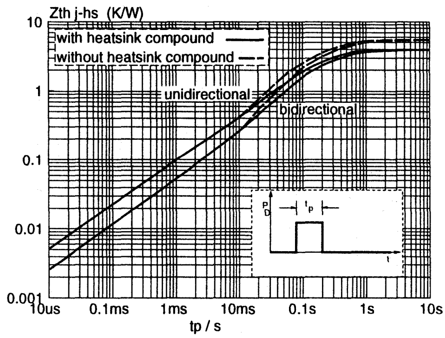


Fig.11. Transient thermal impedance $Z_{th\,j\text{-}hs}$, versus pulse width t_p.

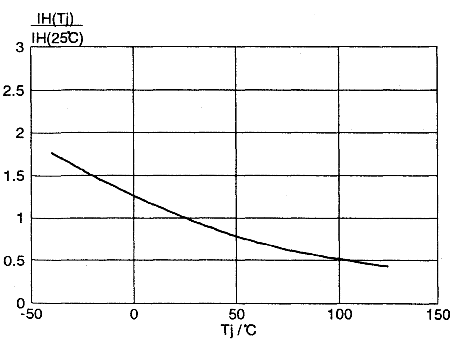


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j.

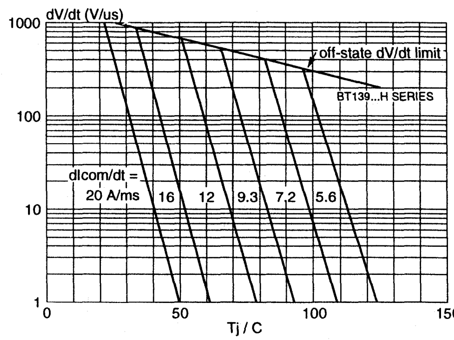


Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation dI_T/dt. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation dI_T/dt.

GENERAL DESCRIPTION

Glass passivated thyristors in a plastic envelope, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

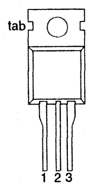
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT145-	500R	600R	800R	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(AV)}$	Average on-state current	16	16	16	A
$I_{T(RMS)}$	RMS on-state current	25	25	25	A
I_{TSM}	Non-repetitive peak on-state current	300	300	300	A

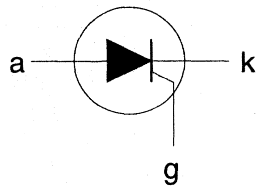
PINNING - TO220AB

PIN	DESCRIPTION
1	cathode
2	anode
3	gate
tab	anode

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500R	-600R	-800R	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(AV)}$	Average on-state current	half sine wave; $T_{mb} \leq 101$ ˚C	-	16			A
$I_{T(RMS)}$	RMS on-state current	all conduction angles	-	25			A
I_{TSM}	Non-repetitive peak on-state current	half sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 10 ms	-	300			A
		t = 8.3 ms	-	330			A
I^2t	I^2t for fusing	t = 10 ms	-	450			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 50$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs	-	200			A/µs
I_{GM}	Peak gate current		-	5			A
V_{GM}	Peak gate voltage		-	5			V
V_{RGM}	Peak reverse gate voltage		-	5			V
P_{GM}	Peak gate power		-	20			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A	-	5	35	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A	-	25	80	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	20	60	mA
V_T	On-state voltage	I_T = 30 A	-	1.1	1.5	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.6	1.0	V
		$V_D = V_{DRM(max)}$; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D, I_R	Off-state leakage current	$V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; T_j = 125 ˚C	-	0.2	1.0	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	200	500	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 40 A; $V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs
t_q	Circuit commutated turn-off time	V_D = 67% $V_{DRM(max)}$; T_j = 125 ˚C; I_{TM} = 50 A; V_R = 25 V; dI_{TM}/dt = 30 A/µs; dV_D/dt = 50 V/µs	-	70	-	µs

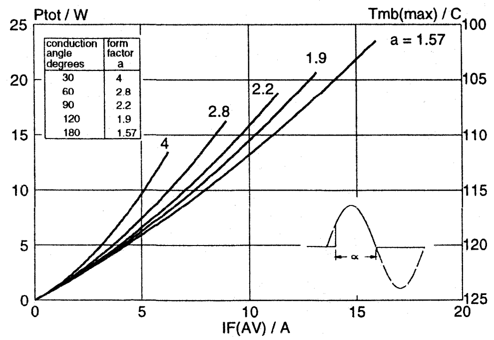


Fig.1. Maximum on-state dissipation, P_{tot}, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}$/ $I_{T(AV)}$.

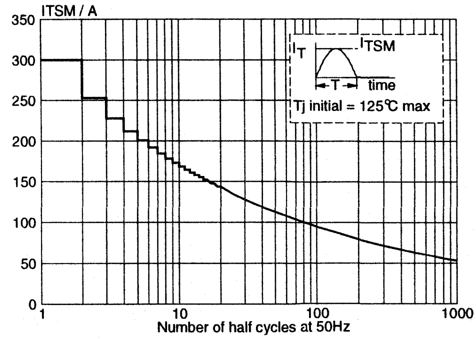


Fig.4. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

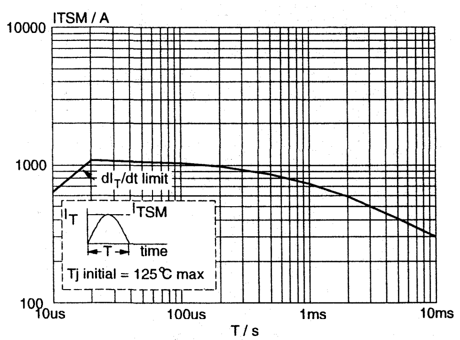


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq$ 10ms.

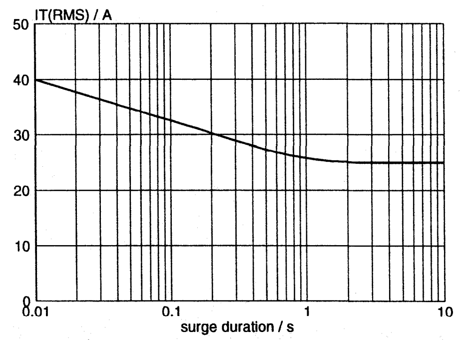


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq$ 101˚C.

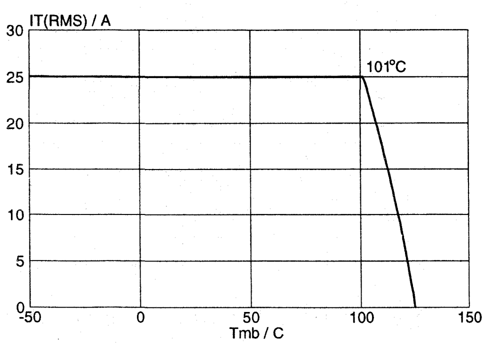


Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

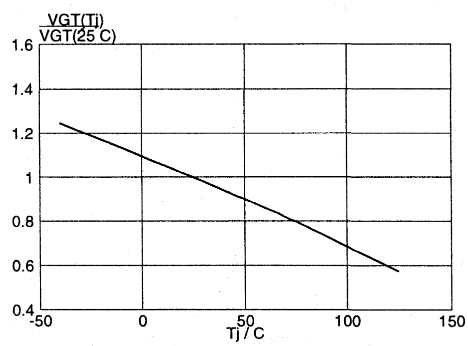


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)$/ V_{GT}(25˚C), versus junction temperature T_j.

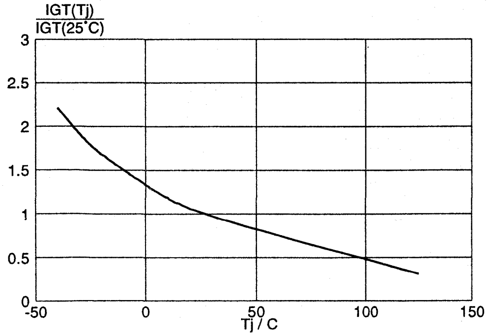


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

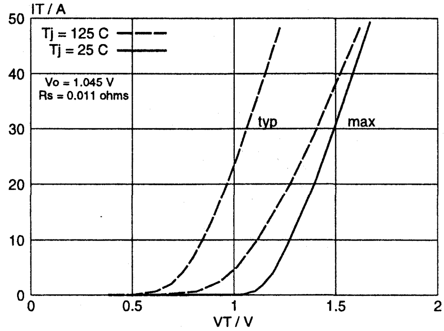


Fig.10. Typical and maximum on-state characteristic.

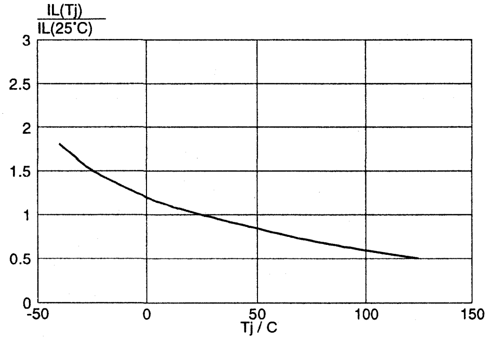


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.

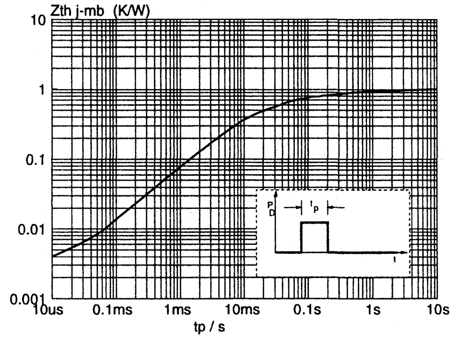


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width t_p.

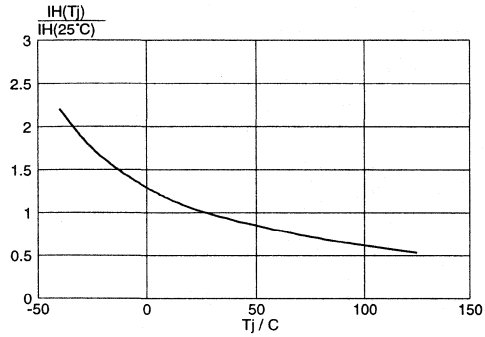


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j.

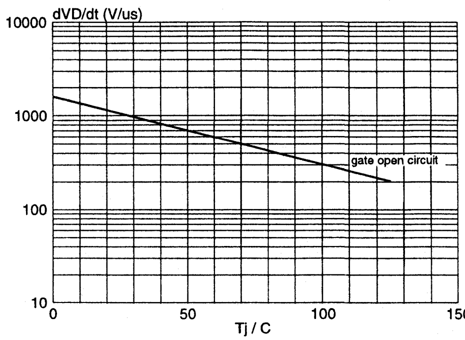


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

Thyristors logic level

BT148 series

GENERAL DESCRIPTION

Glass passivated, sensitive gate thyristors in a plastic envelope, intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

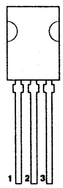
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT148-	400R	500R	600R	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages	400	500	600	V
$I_{T(AV)}$	Average on-state current	2.5	2.5	2.5	A
$I_{T(RMS)}$	RMS on-state current	4	4	4	A
I_{TSM}	Non-repetitive peak on-state current	25	25	25	A

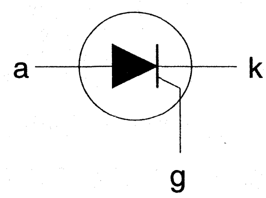
PINNING - SOT82

PIN	DESCRIPTION
1	cathode
2	anode
3	gate
tab	anode

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-400R	-500R	-600R	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages		-	400[1]	500[1]	600[1]	V
$I_{T(AV)}$	Average on-state current	half sine wave; $T_{mb} \leq 113$ ˚C	-	2.5			A
$I_{T(RMS)}$	RMS on-state current	all conduction angles	-	4			A
I_{TSM}	Non-repetitive peak on-state current	half sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 10 ms	-	25			A
		t = 8.3 ms	-	27			A
I^2t	I^2t for fusing	t = 10 ms	-	3.1			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 10$ A; $I_G = 50$ mA; $dI_G/dt = 50$ mA/µs	-	50			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
V_{RGM}	Peak reverse gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A	-	15	200	µA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A	-	0.17	10	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	0.10	6	mA
V_T	On-state voltage	I_T = 5 A	-	1.23	1.8	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.4	1.5	V
		$V_D = V_{DRM(max)}$; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.3	-	V
I_D, I_R	Off-state leakage current	$V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; R_{GK} = 100 Ω	-	50	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 10 A; $V_D = V_{DRM(max)}$; I_G = 5 mA; dI_G/dt = 0.2 A/µs	-	2	-	µs
t_q	Circuit commutated turn-off time	V_D = 67% $V_{DRM(max)}$; T_j = 125 ˚C; I_{TM} = 8 A; V_R = 10 V; dI_{TM}/dt = 10 A/µs; dV_D/dt = 2 V/µs; R_{GK} = 1 kΩ	-	100	-	µs

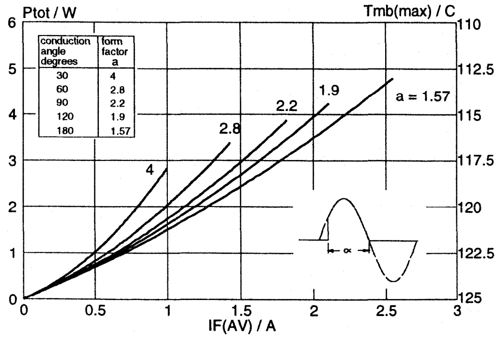


Fig.1. Maximum on-state dissipation, P_{tot}, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}$/ $I_{T(AV)}$.

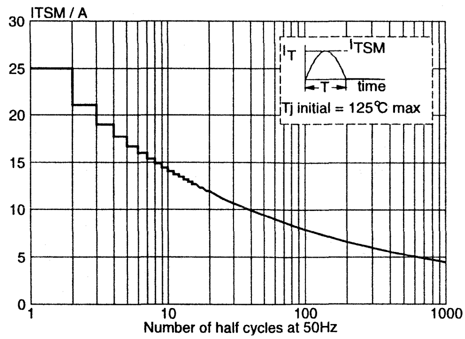


Fig.4. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

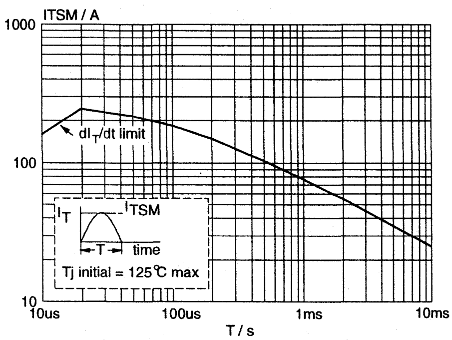


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq$ 10ms.

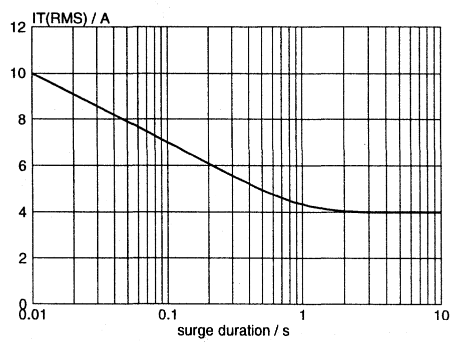


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq$ 113˚C.

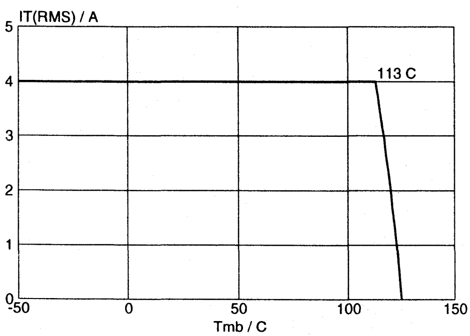


Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

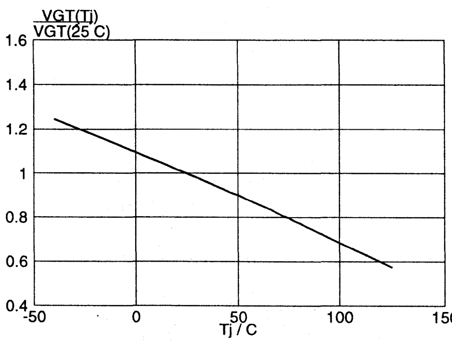


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)$/ V_{GT}(25˚C), versus junction temperature T_j.

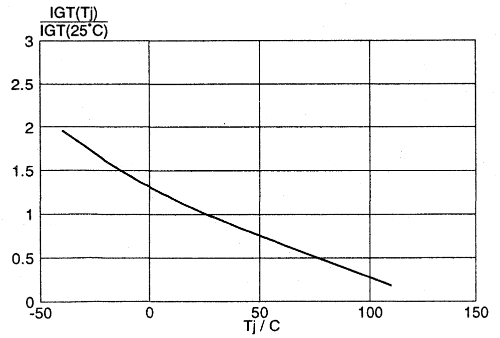


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/I_{GT}(25˚C)$, versus junction temperature T_j.

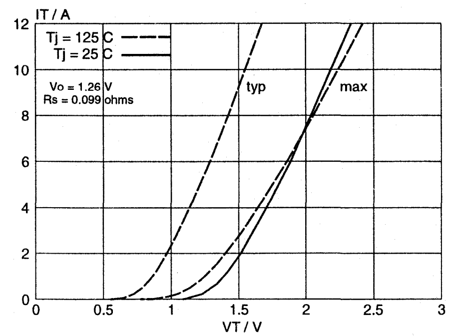


Fig.10. Typical and maximum on-state characteristic.

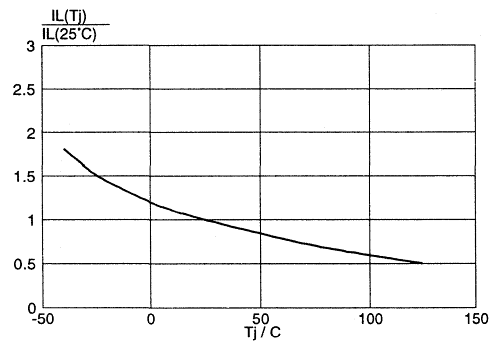


Fig.8. Normalised latching current $I_L(T_j)/I_L(25˚C)$, versus junction temperature T_j.

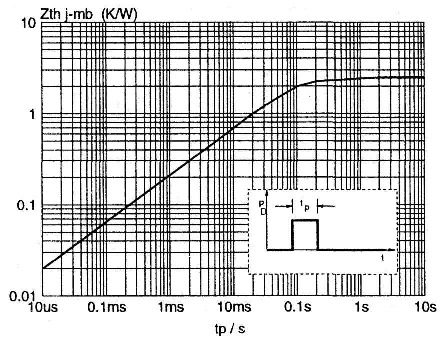


Fig.11. Transient thermal impedance $Z_{th\,j\text{-}mb}$, versus pulse width t_p.

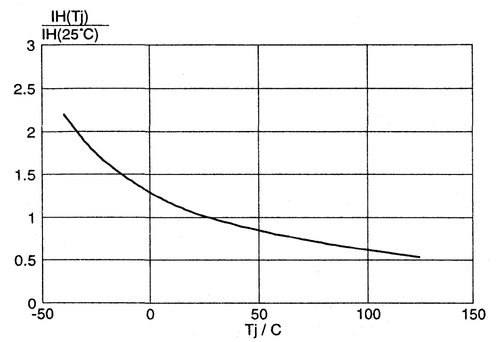


Fig.9. Normalised holding current $I_H(T_j)/I_H(25˚C)$, versus junction temperature T_j.

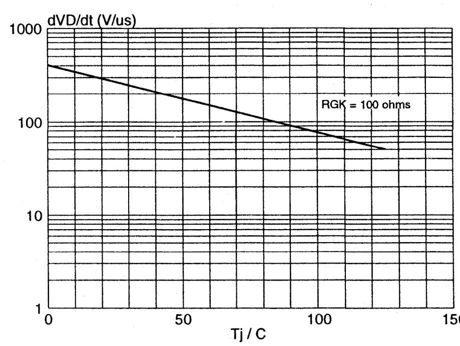


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

Thyristors logic level

BT148W series

GENERAL DESCRIPTION

Glass passivated, sensitive gate thyristors in a plastic envelope suitable for surface mounting, intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

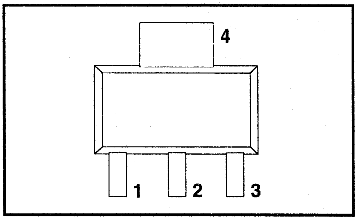
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT148W-	400R	500R	600R	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages	400	500	600	V
$I_{T(AV)}$	Average on-state current	0.6	0.6	0.6	A
$I_{T(RMS)}$	RMS on-state current	1	1	1	A
I_{TSM}	Non-repetitive peak on-state current	10	10	10	A

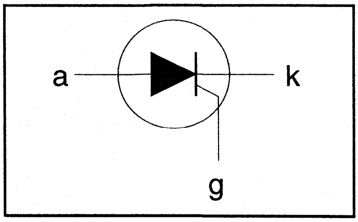
PINNING - SOT223

PIN	DESCRIPTION
1	cathode
2	anode
3	gate
tab	anode

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-400R	-500R	-600R	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages		-	400[1]	500[1]	600[1]	V
$I_{T(AV)}$	Average on-state current	half sine wave; $T_{sp} \leq 112$ ˚C	-	0.6			A
$I_{T(RMS)}$	RMS on-state current	all conduction angles	-	1			A
I_{TSM}	Non-repetitive peak on-state current	half sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 10 ms	-	10			A
		t = 8.3 ms	-	11			A
I^2t	I^2t for fusing	t = 10 ms	-	0.5			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 4$ A; $I_G = 200$ mA; $dI_G/dt = 200$ mA/µs	-	50			A/µs
I_{GM}	Peak gate current		-	1			A
V_{GM}	Peak gate voltage		-	5			V
V_{RGM}	Peak reverse gate voltage		-	5			V
P_{GM}	Peak gate power		-	1.2			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.12			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}sp}$	Thermal resistance junction to solder point		-	-	15	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	pcb mounted, minimum footprint	-	156	-	K/W
		pcb mounted, pad area as in fig:14	-	70	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A	-	50	200	µA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A	-	0.17	10	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	0.10	6	mA
V_T	On-state voltage	I_T = 2 A	-	1.3	1.5	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.4	1.5	V
		$V_R = V_{RRM(max)}$; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.3	-	V
I_D, I_R	Off-state leakage current	$V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; R_{GK} = 100 Ω	-	50	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 4 A; $V_D = V_{DRM(max)}$; I_G = 5 mA; dI_G/dt = 0.2 A/µs	-	2	-	µs
t_q	Circuit commutated turn-off time	V_D = 67% $V_{DRM(max)}$; T_j = 125 ˚C; I_{TM} = 2 A; V_R = 35 V; dI_{TM}/dt = 30 A/µs; dV_D/dt = 2 V/µs; R_{GK} = 1 kΩ	-	100	-	µs

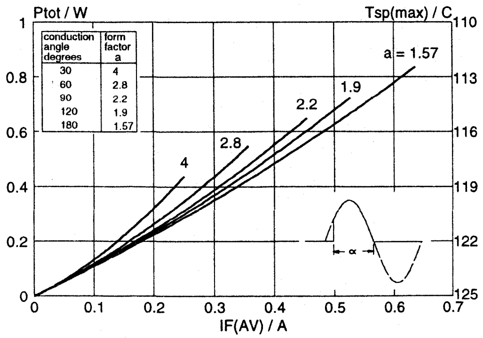


Fig.1. Maximum on-state dissipation, P_{tot}, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}/I_{T(AV)}$.

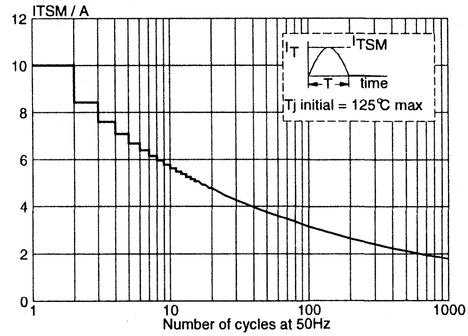


Fig.4. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

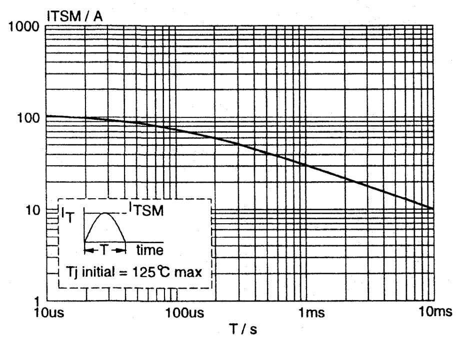


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 10ms$.

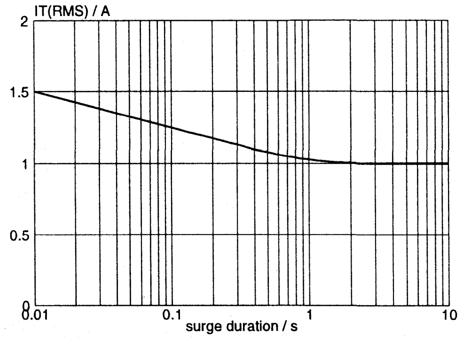


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{sp} \leq 112˚C$.

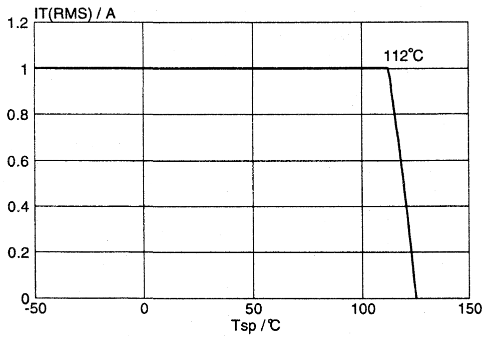


Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus solder point temperature T_{sp}.

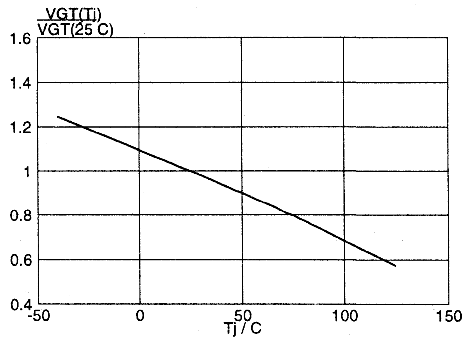


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25˚C)$, versus junction temperature T_j.

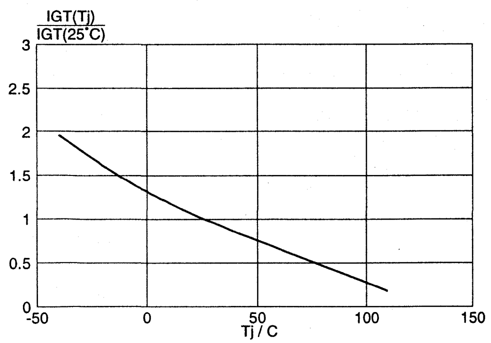


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/\ I_{GT}(25^{\circ}C)$, versus junction temperature T_j.

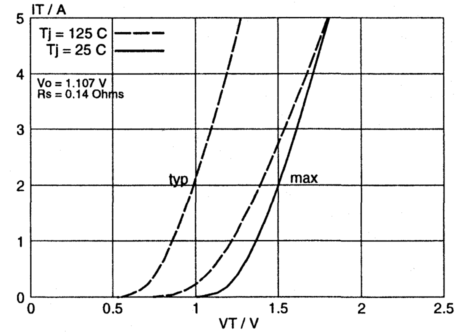


Fig.10. Typical and maximum on-state characteristic.

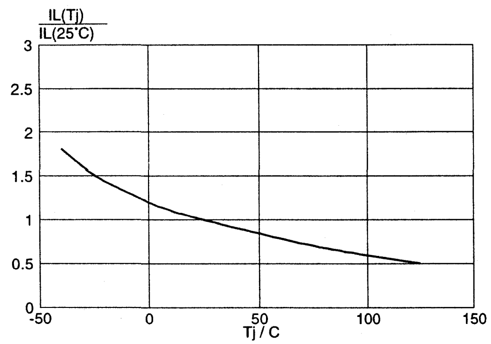


Fig.8. Normalised latching current $I_L(T_j)/\ I_L(25^{\circ}C)$, versus junction temperature T_j.

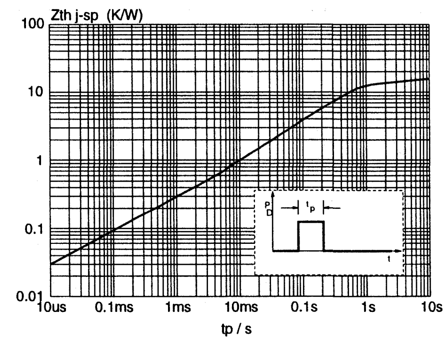


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}sp}$, versus pulse width t_p.

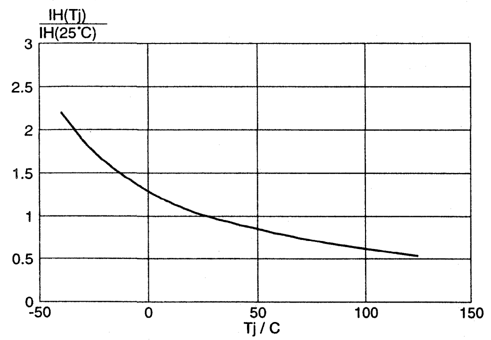


Fig.9. Normalised holding current $I_H(T_j)/\ I_H(25^{\circ}C)$, versus junction temperature T_j.

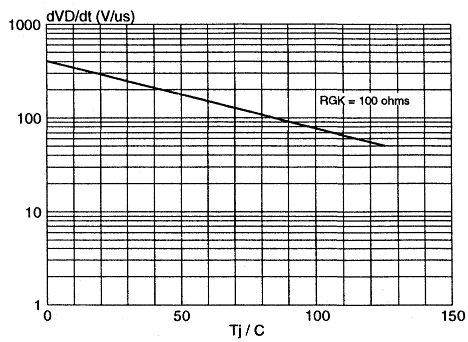


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

MOUNTING INSTRUCTIONS

Dimensions in mm.

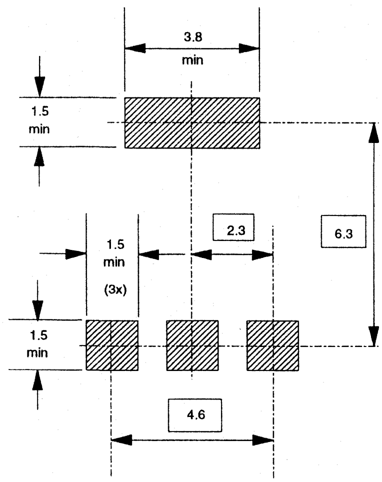


Fig.13. soldering pattern for surface mounting SOT223.

PRINTED CIRCUIT BOARD

Dimensions in mm.

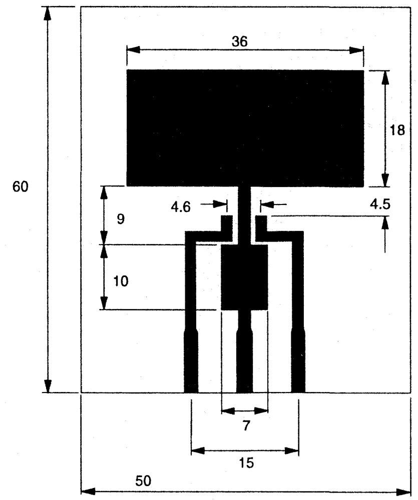


Fig.14. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 µm thick).

GENERAL DESCRIPTION

Glass passivated, sensitive gate thyristors in a plastic envelope, intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

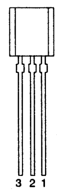
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	MAX.	UNIT
	BT149	B	D	E	G	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages	200	400	500	600	V
$I_{T(AV)}$	Average on-state current	0.5	0.5	0.5	0.5	A
$I_{T(RMS)}$	RMS on-state current	0.8	0.8	0.8	0.8	A
I_{TSM}	Non-repetitive peak on-state current	8	8	8	8	A

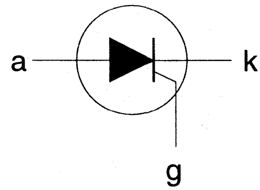
PINNING - TO92 variant

PIN	DESCRIPTION
1	cathode
2	gate
3	anode

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.				UNIT
				B	D	E	G	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages		-	200[1]	400[1]	500[1]	600[1]	V
$I_{T(AV)}$	Average on-state current	half sine wave; $T_{lead} \leq 83$ ˚C	-	0.5				A
$I_{T(RMS)}$	RMS on-state current	all conduction angles	-	0.8				A
I_{TSM}	Non-repetitive peak on-state current	t = 10 ms	-	8				A
		t = 8.3 ms	-	9				A
		half sine wave; T_j = 125 ˚C prior to surge; with reapplied $V_{DRM(max)}$						
I^2t	I^2t for fusing	t = 10 ms	-	0.32				A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	I_{TM} = 2 A; I_G = 10 mA; dI_G/dt = 100 mA/μs	-	50				A/μs
I_{GM}	Peak gate current		-	1				A
V_{GM}	Peak gate voltage		-	5				V
V_{RGM}	Peak reverse gate voltage		-	5				V
P_{GM}	Peak gate power		-	2				W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.1				W
T_{stg}	Storage temperature		-40	150				˚C
T_j	Operating junction temperature		-	125				˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/μs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}lead}$	Thermal resistance junction to lead		-	-	60	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	pcb mounted; lead length = 4mm	-	150	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 10 mA; gate open circuit	-	50	200	µA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.5 mA; R_{GK} = 1 kΩ	-	2	6	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.5 mA; R_{GK} = 1 kΩ	-	2	5	mA
V_T	On-state voltage	I_T = 1 A	-	1.2	1.35	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 10 mA; gate open circuit	-	0.5	0.8	V
		$V_D = V_{DRM(max)}$; I_T = 10 mA; T_j = 125 ˚C; gate open circuit	0.2	0.3	-	V
I_D, I_R	Off-state leakage current	$V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; T_j = 125 ˚C; R_{GK} = 1 kΩ	-	0.05	0.1	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; R_{GK} = 1 kΩ	-	25	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 2 A; $V_D = V_{DRM(max)}$; I_G = 10 mA; dI_G/dt = 0.1 A/µs	-	2	-	µs
t_q	Circuit commutated turn-off time	V_D = 67% $V_{DRM(max)}$; T_j = 125 ˚C; I_{TM} = 1.6 A; V_R = 35 V; dI_{TM}/dt = 30 A/µs; dV_D/dt = 2 V/µs; R_{GK} = 1 kΩ	-	100	-	µs

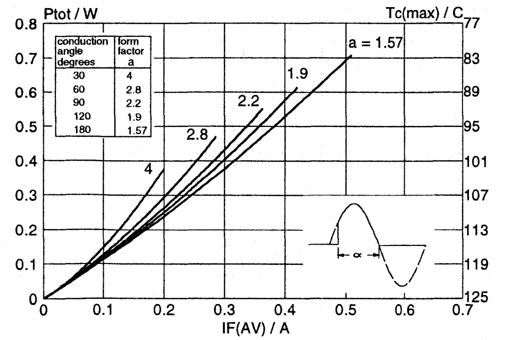


Fig.1. Maximum on-state dissipation, P_{tot}, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}$/ $I_{T(AV)}$.

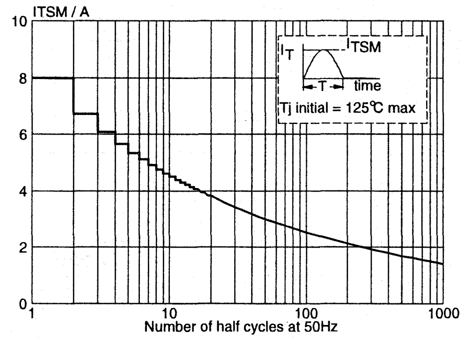


Fig.4. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

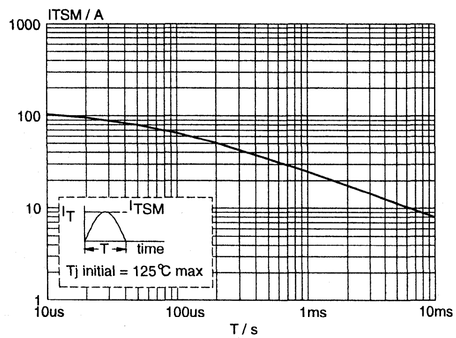


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq$ 10ms.

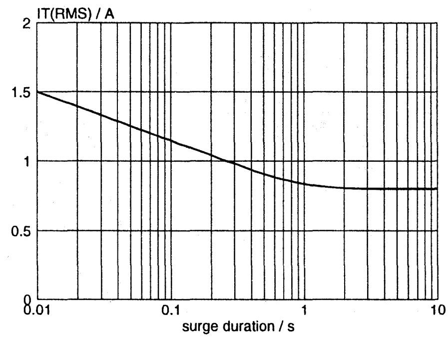


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{lead} \leq$ 83˚C.

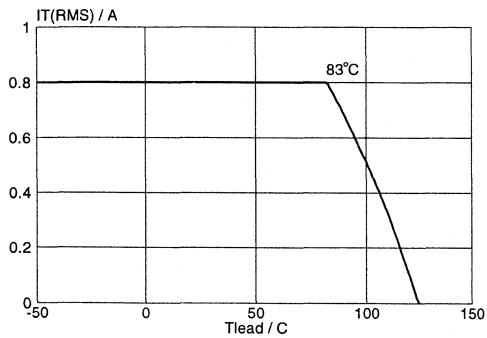


Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus lead temperature, T_{lead}.

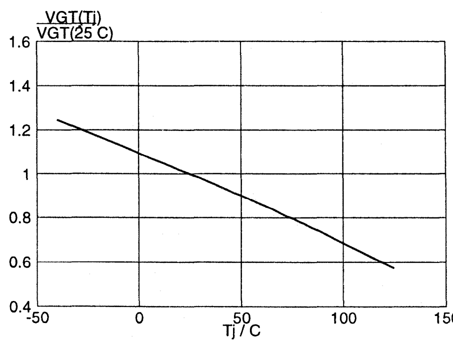


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)$/ V_{GT}(25˚C), versus junction temperature T_j.

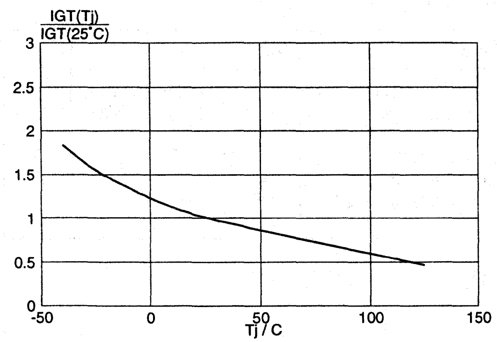


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/\ I_{GT}(25^{\circ}C)$, versus junction temperature T_j.

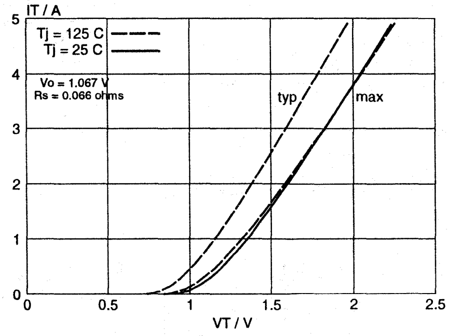


Fig.10. Typical and maximum on-state characteristic.

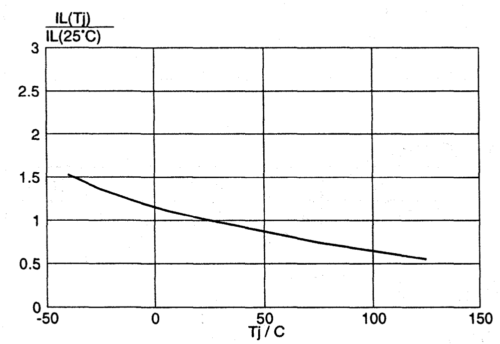


Fig.8. Normalised latching current $I_L(T_j)/\ I_L(25^{\circ}C)$, versus junction temperature T_j, $R_{GK} = 1\ k\Omega$.

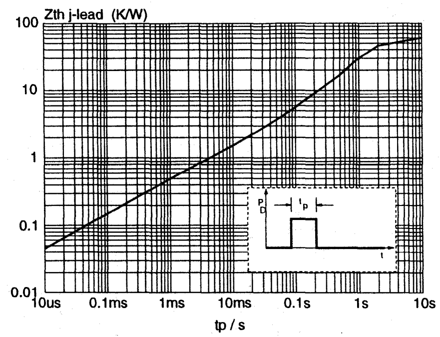


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}lead}$, versus pulse width t_p.

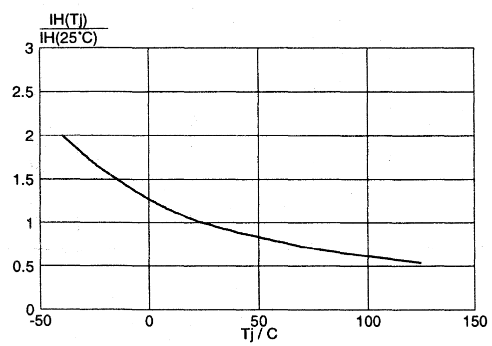


Fig.9. Normalised holding current $I_H(T_j)/\ I_H(25^{\circ}C)$, versus junction temperature T_j, $R_{GK} = 1\ k\Omega$.

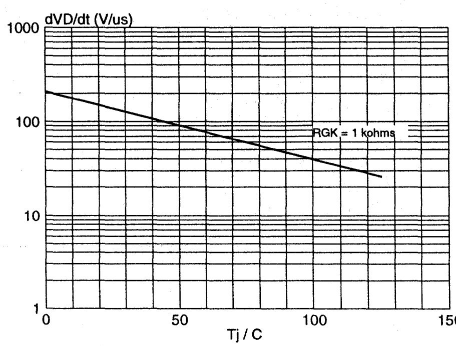


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

GENERAL DESCRIPTION

Glass passivated, sensitive gate thyristors in a plastic envelope, intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

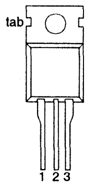
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT150-	500R	600R	800R	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(AV)}$	Average on-state current	2.5	2.5	2.5	A
$I_{T(RMS)}$	RMS on-state current	4	4	4	A
I_{TSM}	Non-repetitive peak on-state current	25	25	25	A

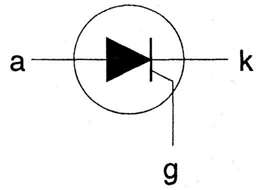
PINNING - TO220AB

PIN	DESCRIPTION
1	cathode
2	anode
3	gate
tab	anode

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500R	-600R	-800R	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(AV)}$	Average on-state current	half sine wave; $T_{mb} \leq 113$ ˚C	-	2.5			A
$I_{T(RMS)}$	RMS on-state current	all conduction angles	-	4			A
I_{TSM}	Non-repetitive peak on-state current	half sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 10 ms	-	25			A
		t = 8.3 ms	-	27			A
I^2t	I^2t for fusing	t = 10 ms	-	3.1			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 10$ A; $I_G = 50$ mA; $dI_G/dt = 50$ mA/µs	-	50			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
V_{RGM}	Peak reverse gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A	-	15	200	µA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A	-	0.17	10	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	0.10	6	mA
V_T	On-state voltage	I_T = 5 A	-	1.23	1.8	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.4	1.5	V
		$V_D = V_{DRM(max)}$; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.3	-	V
I_D, I_R	Off-state leakage current	$V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; R_{GK} = 100 Ω	-	50	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 10 A; $V_D = V_{DRM(max)}$; I_G = 5 mA; dI_G/dt = 0.2 A/µs	-	2	-	µs
t_q	Circuit commutated turn-off time	V_D = 67% $V_{DRM(max)}$; T_j = 125 ˚C; I_{TM} = 8 A; V_R = 10 V; dI_{TM}/dt = 10 A/µs; dV_D/dt = 2 V/µs; R_{GK} = 1 kΩ	-	100	-	µs

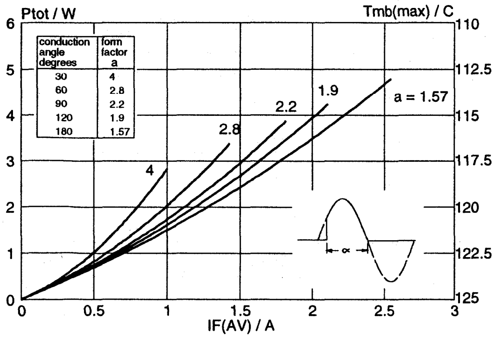


Fig.1. Maximum on-state dissipation, P_{tot}, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}$/ $I_{T(AV)}$.

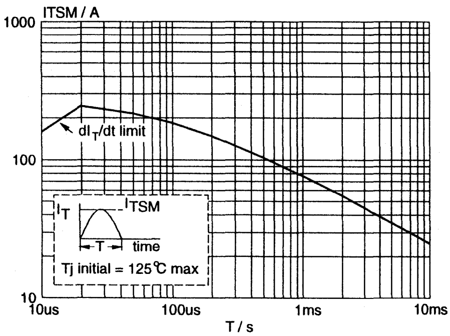


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq$ 10ms.

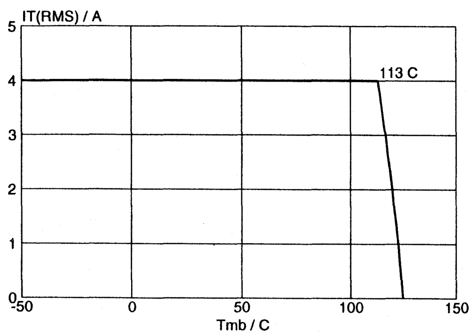


Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

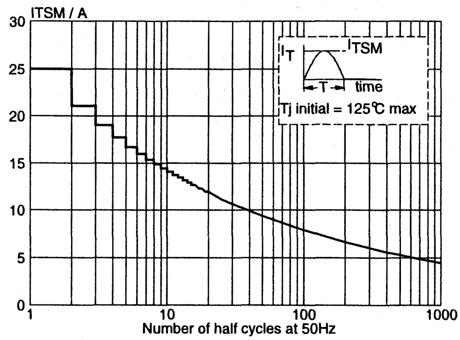


Fig.4. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

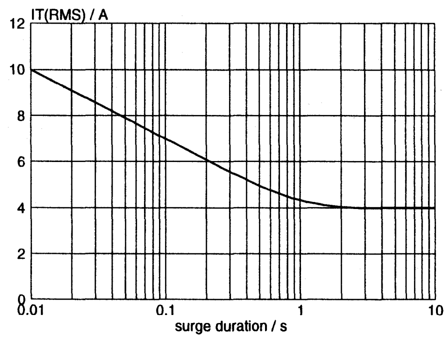


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq$ 113˚C.

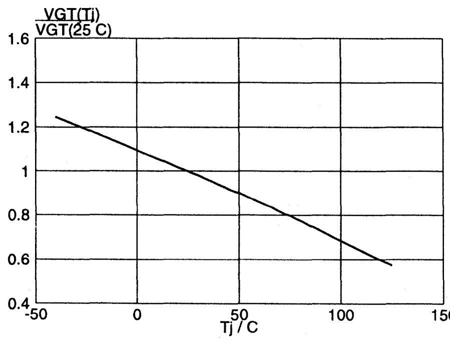


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)$/ V_{GT}(25˚C), versus junction temperature T_j.

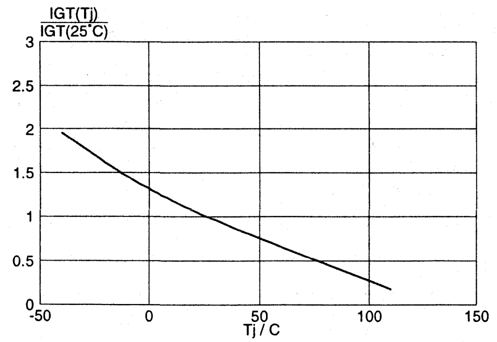


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

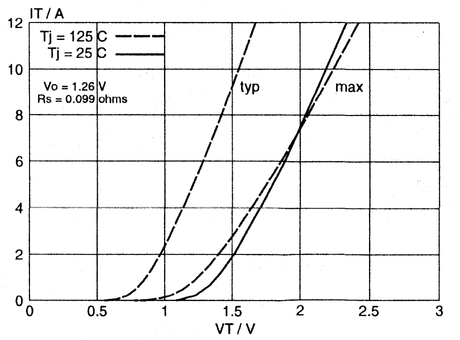


Fig.10. Typical and maximum on-state characteristic.

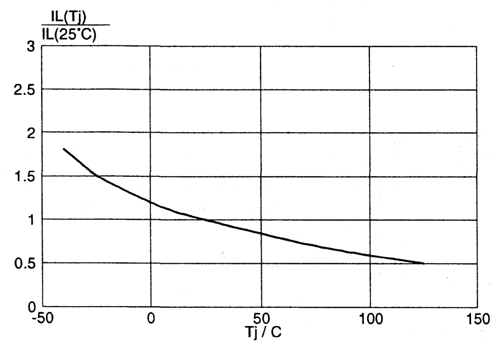


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.

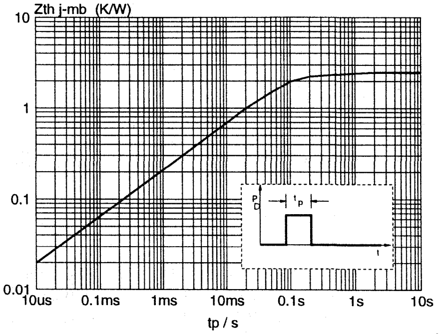


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width t_p.

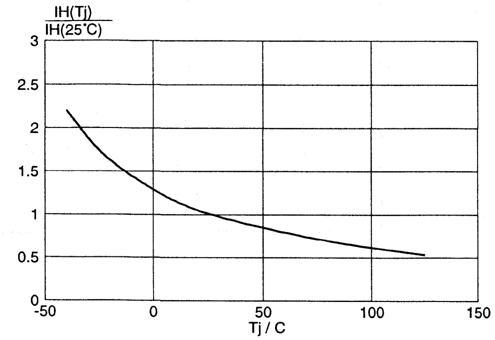


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j.

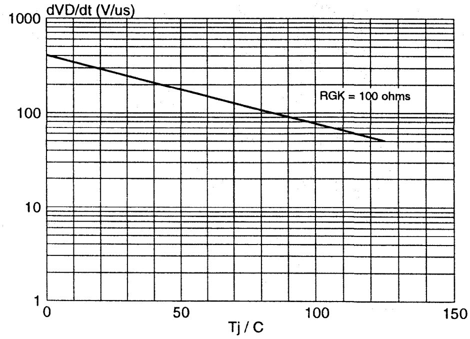


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

GENERAL DESCRIPTION

Glass passivated thyristors in a plastic envelope, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

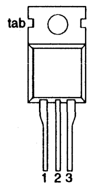
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT151-	500R	650R	800R	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages	500	650	800	V
$I_{T(AV)}$	Average on-state current	7.5	7.5	7.5	A
$I_{T(RMS)}$	RMS on-state current	12	12	12	A
I_{TSM}	Non-repetitive peak on-state current	100	100	100	A

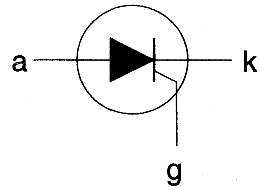
PINNING - TO220AB

PIN	DESCRIPTION
1	cathode
2	anode
3	gate
tab	anode

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500R	-650R	-800R	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages		-	500[1]	650[1]	800	V
$I_{T(AV)}$	Average on-state current	half sine wave; $T_{mb} \leq 109$ ˚C	-	7.5			A
$I_{T(RMS)}$	RMS on-state current	all conduction angles	-	12			A
I_{TSM}	Non-repetitive peak on-state current	half sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 10 ms	-	100			A
		t = 8.3 ms	-	110			A
I^2t	I^2t for fusing	t = 10 ms	-	50			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 20$ A; $I_G = 50$ mA; $dI_G/dt = 50$ mA/µs	-	50			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
V_{RGM}	Peak reverse gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\,j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.3	K/W
$R_{th\,j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A	-	2	15	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A	-	10	40	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	7	20	mA
V_T	On-state voltage	I_T = 23 A	-	1.4	1.75	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.6	1.5	V
		$V_D = V_{DRM(max)}$; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D, I_R	Off-state leakage current	$V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform;				
		Gate open circuit	50	130	-	V/µs
		R_{GK} = 100 Ω	200	1000	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 40 A; $V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs
t_q	Circuit commutated turn-off time	V_D = 67% $V_{DRM(max)}$; T_j = 125 ˚C; I_{TM} = 20 A; V_R = 25 V; dI_{TM}/dt = 30 A/µs; dV_D/dt = 50 V/µs; R_{GK} = 100 Ω	-	70	-	µs

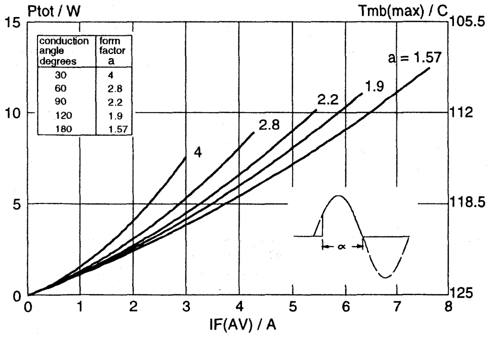


Fig.1. Maximum on-state dissipation, P_{tot}, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}/I_{T(AV)}$.

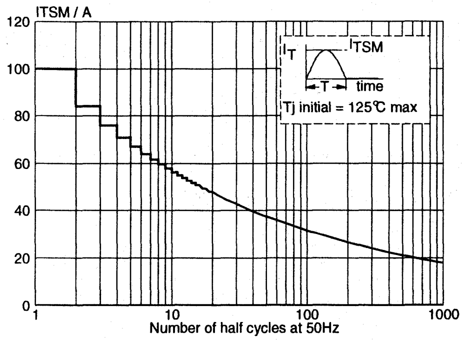


Fig.4. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

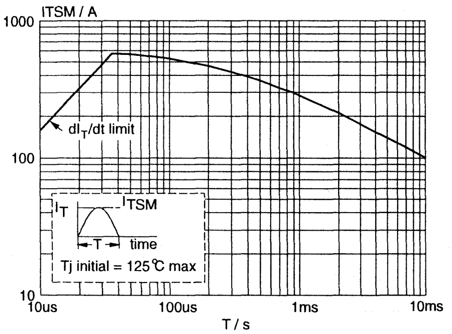


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq$ 10ms.

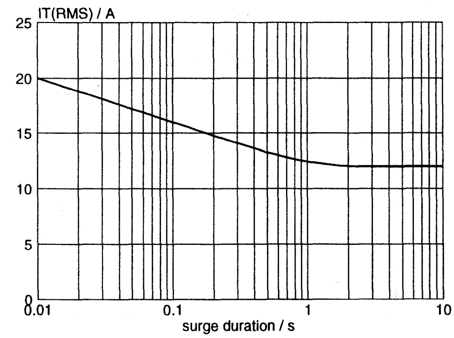


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq$ 109˚C.

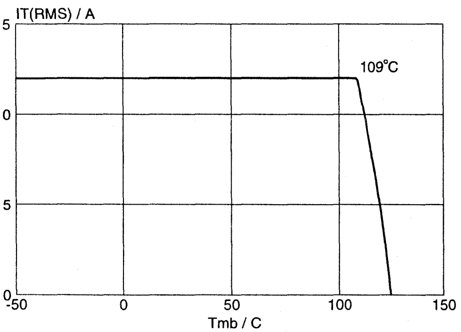


Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

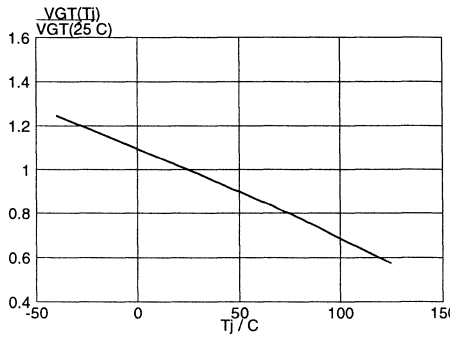


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25˚C)$, versus junction temperature T_j.

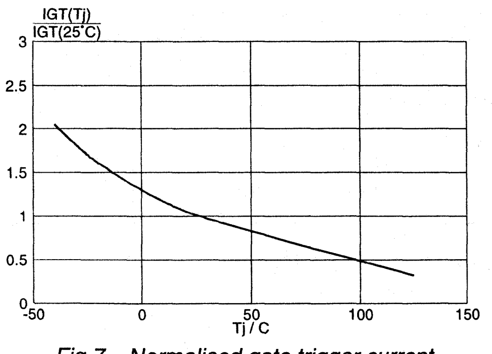


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

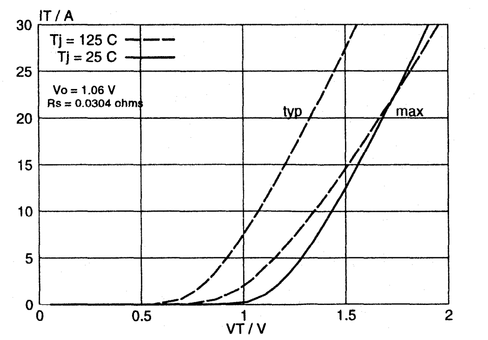


Fig.10. Typical and maximum on-state characteristic.

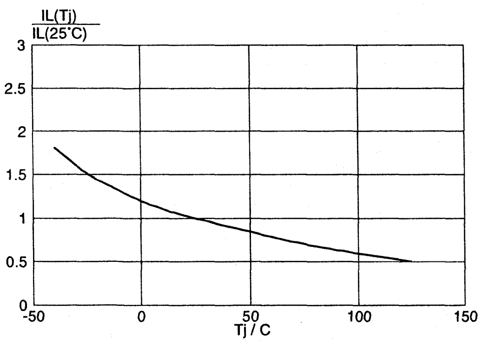


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.

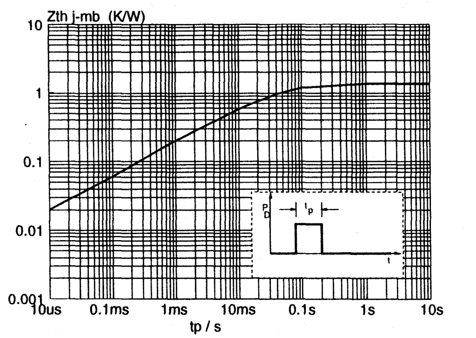


Fig.11. Transient thermal impedance $Z_{th\,j\text{-}mb}$, versus pulse width t_p.

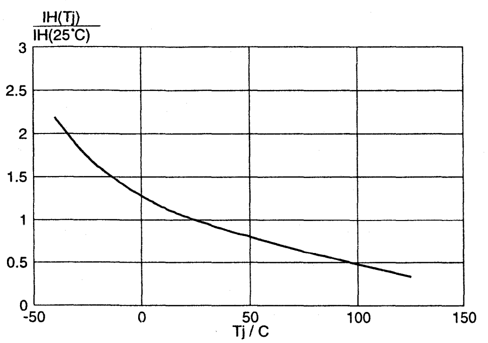


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j.

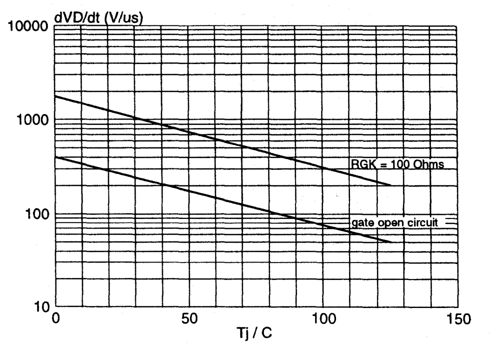


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

GENERAL DESCRIPTION

Glass passivated thyristors in a full pack, plastic envelope, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

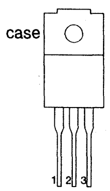
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT151F-	**500**	**650**	**800**	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages	500	650	800	V
$I_{T(AV)}$	Average on-state current	5.7	5.7	5.7	A
$I_{T(RMS)}$	RMS on-state current	9	9	9	A
I_{TSM}	Non-repetitive peak on-state current	100	100	100	A

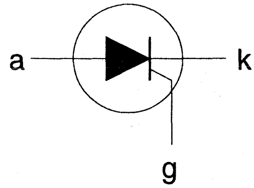
PINNING - SOT186

PIN	DESCRIPTION
1	cathode
2	anode
3	gate
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	**-650**	**-800**	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages		-	500[1]	650[1]	800	V
$I_{T(AV)}$	Average on-state current	half sine wave; $T_{hs} \leq 87$ ˚C	-	5.7			A
$I_{T(RMS)}$	RMS on-state current	all conduction angles	-	9			A
I_{TSM}	Non-repetitive peak on-state current	half sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 10 ms	-	100			A
		t = 8.3 ms	-	110			A
I^2t	I^2t for fusing	t = 10 ms	-	50			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 20$ A; $I_G = 50$ mA; $dI_G/dt = 50$ mA/μs	-	50			A/μs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
V_{RGM}	Peak reverse gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/μs.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	4.5	K/W
		without heatsink compound	-	-	6.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A	-	2	15	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A	-	10	40	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	7	20	mA
V_T	On-state voltage	I_T = 23 A	-	1.4	1.75	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.6	1.5	V
		$V_D = V_{DRM(max)}$; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D, I_R	Off-state leakage current	$V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform				
		Gate open circuit	50	130	-	V/µs
		R_{GK} = 100 Ω	200	1000	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 40 A; $V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs
t_q	Circuit commutated turn-off time	V_D = 67% $V_{DRM(max)}$; T_j = 125 ˚C; I_{TM} = 20 A; V_R = 25 V; dI_{TM}/dt = 30 A/µs; dV_D/dt = 50 V/µs; R_{GK} = 100 Ω	-	70	-	µs

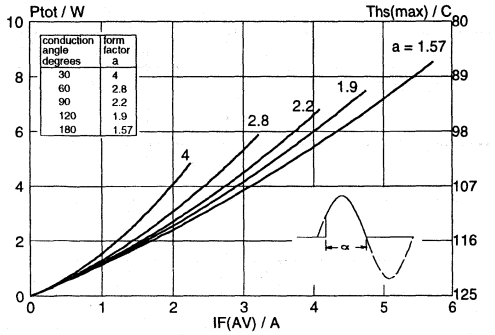


Fig.1. Maximum on-state dissipation, P_{tot}, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}$/ $I_{T(AV)}$.

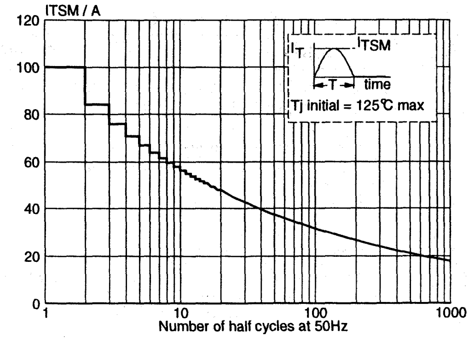


Fig.4. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

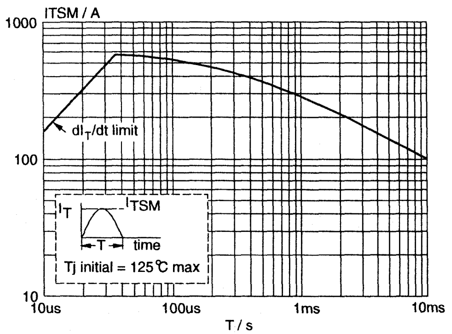


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq$ 10ms.

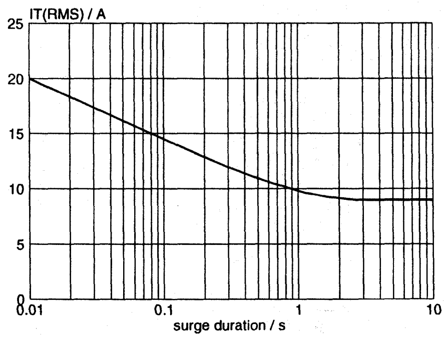


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq$ 87˚C.

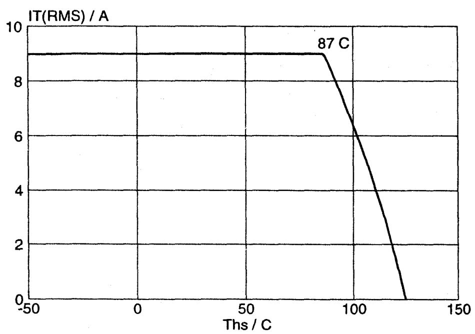


Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature T_{hs}.

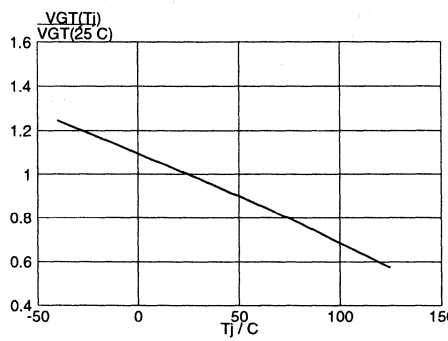


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)$/ V_{GT}(25˚C), versus junction temperature T_j.

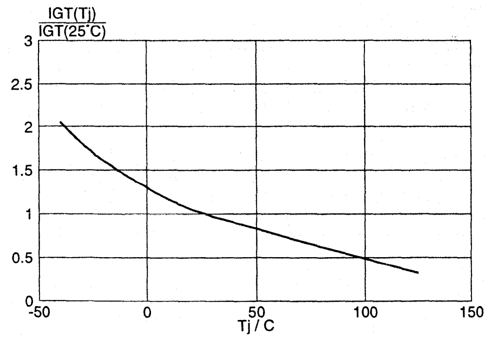


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

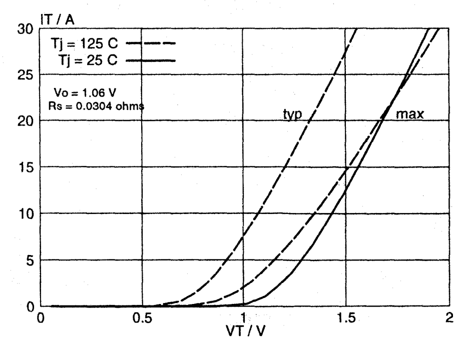


Fig.10. Typical and maximum on-state characteristic.

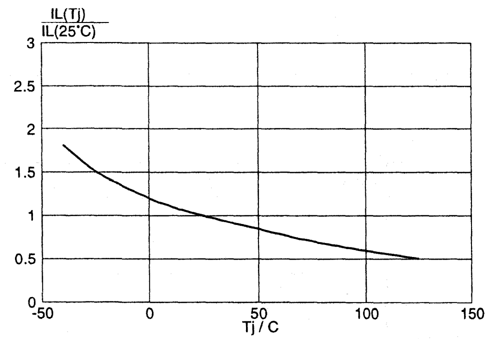


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.

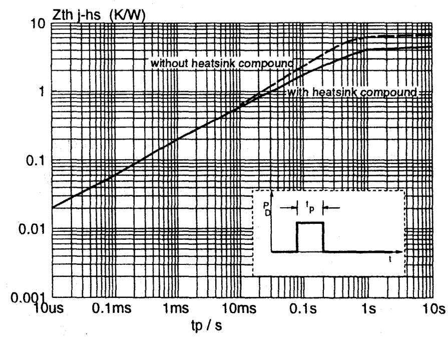


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}hs}$, versus pulse width t_p.

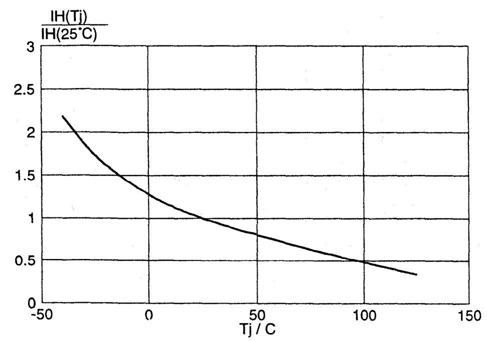


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j.

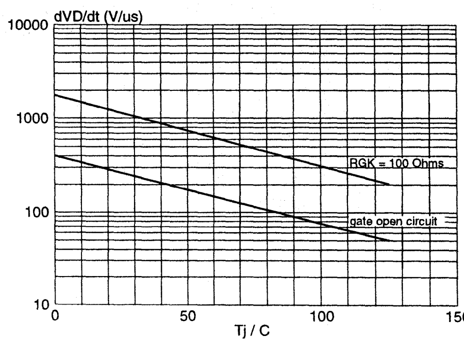


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

GENERAL DESCRIPTION

Glass passivated thyristors in a full pack, plastic envelope, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

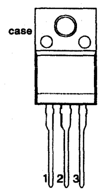
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT151X-	**500**	**650**	**800**	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages	500	650	800	V
$I_{T(AV)}$	Average on-state current	5.7	5.7	5.7	A
$I_{T(RMS)}$	RMS on-state current	9	9	9	A
I_{TSM}	Non-repetitive peak on-state current	100	100	100	A

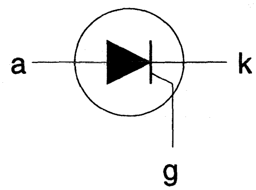
PINNING - SOT186A

PIN	DESCRIPTION
1	cathode
2	anode
3	gate
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	**-650**	**-800**	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages		-	500[1]	650[1]	800	V
$I_{T(AV)}$	Average on-state current	half sine wave; $T_{hs} \leq 87$ ˚C	-	5.7			A
$I_{T(RMS)}$	RMS on-state current	all conduction angles	-	9			A
I_{TSM}	Non-repetitive peak on-state current	half sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 10 ms	-	100			A
		t = 8.3 ms	-	110			A
I^2t	I^2t for fusing	t = 10 ms	-	50			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 20$ A; $I_G = 50$ mA; $dI_G/dt = 50$ mA/μs	-	50			A/μs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
V_{RGM}	Peak reverse gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/μs.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	4.5	K/W
		without heatsink compound	-	-	6.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A	-	2	15	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A	-	10	40	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	7	20	mA
V_T	On-state voltage	I_T = 23 A	-	1.4	1.75	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.6	1.5	V
		$V_D = V_{DRM(max)}$; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D, I_R	Off-state leakage current	$V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform				
		Gate open circuit	50	130	-	V/µs
		R_{GK} = 100 Ω	200	1000	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 40 A; $V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs
t_q	Circuit commutated turn-off time	V_D = 67% $V_{DRM(max)}$; T_j = 125 ˚C; I_{TM} = 20 A; V_R = 25 V; dI_{TM}/dt = 30 A/µs; dV_D/dt = 50 V/µs; R_{GK} = 100 Ω	-	70	-	µs

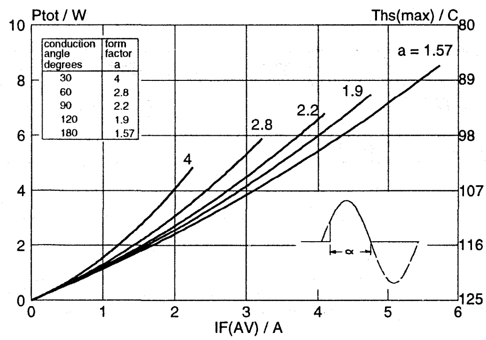


Fig.1. Maximum on-state dissipation, P_{tot}, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}$/ $I_{T(AV)}$.

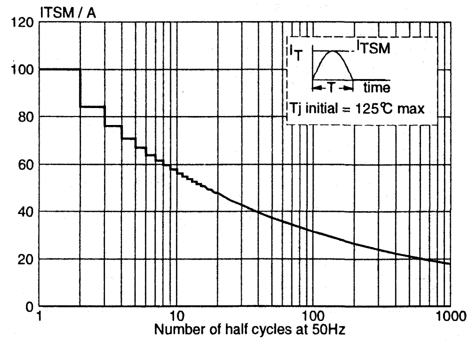


Fig.4. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

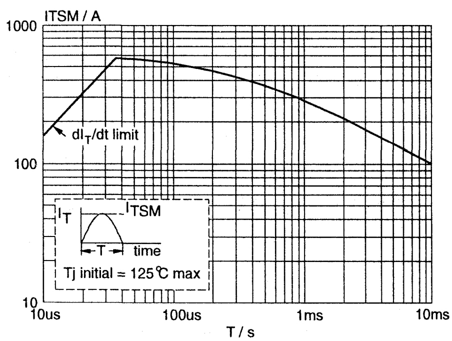


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq$ 10ms.

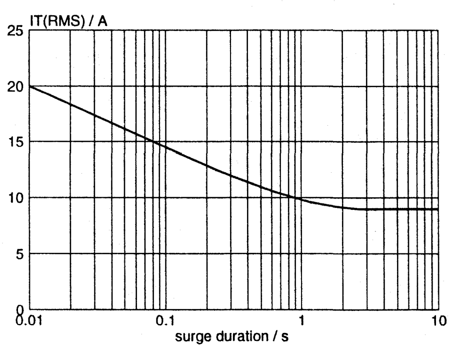


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 87^{\circ}C$.

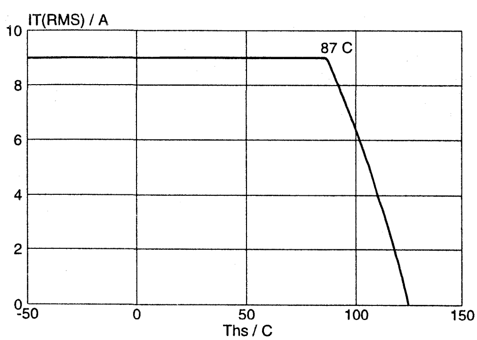


Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature T_{hs}.

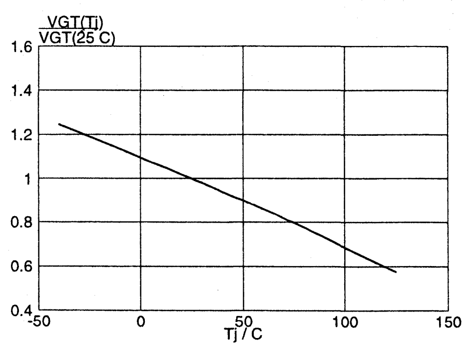


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)$/ $V_{GT}(25^{\circ}C)$, versus junction temperature T_j.

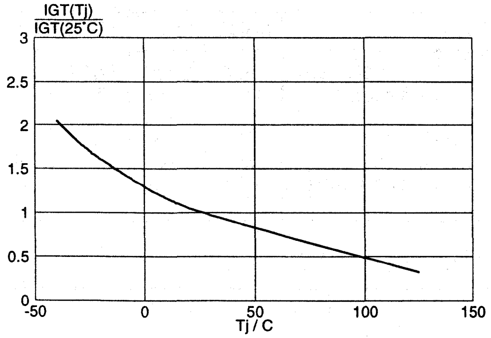


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25^{\circ}C)$, versus junction temperature T_j.

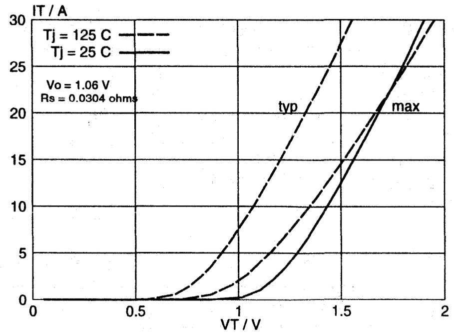


Fig.10. Typical and maximum on-state characteristic.

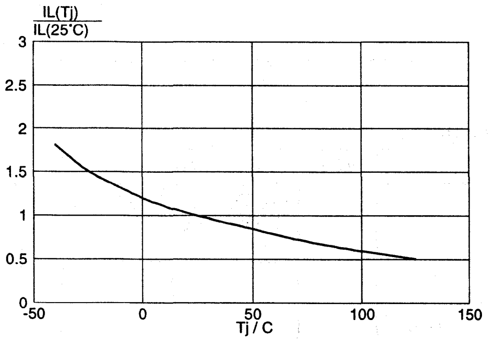


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25^{\circ}C)$, versus junction temperature T_j.

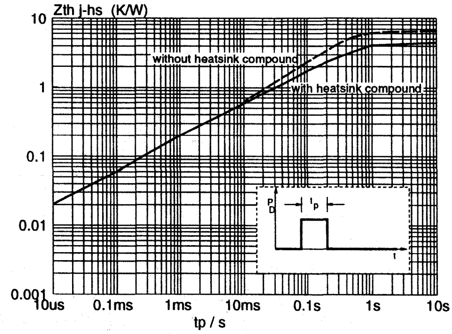


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}hs}$, versus pulse width t_p.

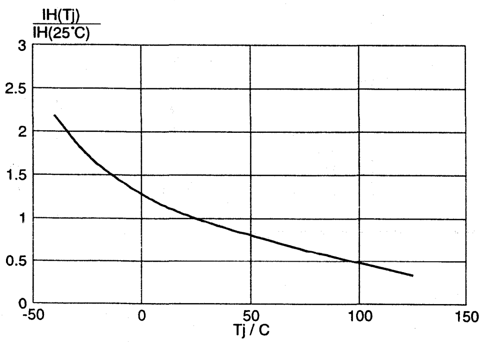


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25^{\circ}C)$, versus junction temperature T_j.

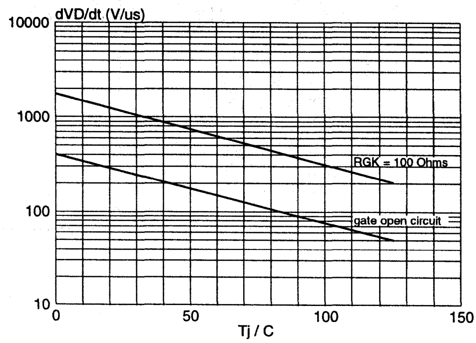


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

GENERAL DESCRIPTION

Glass passivated thyristors in a plastic envelope, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

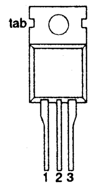
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT152-	500R	600R	800R	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(AV)}$	Average on-state current	13	13	13	A
$I_{T(RMS)}$	RMS on-state current	20	20	20	A
I_{TSM}	Non-repetitive peak on-state current	200	200	200	A

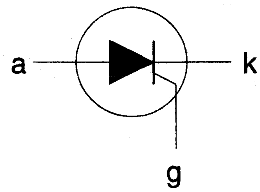
PINNING - TO220AB

PIN	DESCRIPTION
1	cathode
2	anode
3	gate
tab	anode

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500R	-600R	-800R	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(AV)}$	Average on-state current	half sine wave; $T_{mb} \leq 103$ ˚C	-	13			A
$I_{T(RMS)}$	RMS on-state current	all conduction angles	-	20			A
I_{TSM}	Non-repetitive peak on-state current	half sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 10 ms	-	200			A
		t = 8.3 ms	-	220			A
I^2t	I^2t for fusing	t = 10 ms	-	200			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 50$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs	-	200			A/µs
I_{GM}	Peak gate current		-	5			A
V_{GM}	Peak gate voltage		-	5			V
V_{RGM}	Peak reverse gate voltage		-	5			V
P_{GM}	Peak gate power		-	20			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.1	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A	-	3	32	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A	-	25	80	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	15	60	mA
V_T	On-state voltage	I_T = 40 A	-	1.4	1.75	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.6	1.5	V
		$V_D = V_{DRM(max)}$; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D, I_R	Off-state leakage current	$V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; T_j = 125 ˚C	-	0.2	1.0	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform gate open circuit	200	300	-	V/µs
t_{gt}	Gate controlled turn-on time	$V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs; I_{TM} = 40 A	-	2	-	µs
t_q	Circuit commutated turn-off time	V_D = 67% $V_{DRM(max)}$; T_j = 125 ˚C; I_{TM} = 50 A; V_R = 25 V; dI_{TM}/dt = 30 A/µs; dV_D/dt = 50 V/µs; R_{GK} = 100 Ω	-	70	-	µs

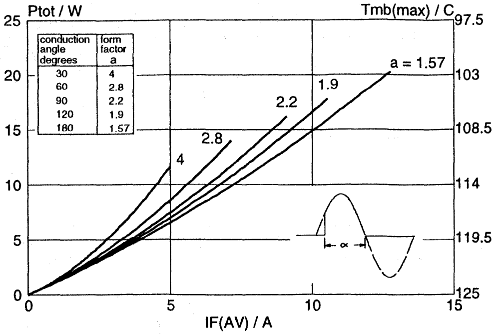


Fig.1. Maximum on-state dissipation, P_{tot}, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}$/ $I_{T(AV)}$.

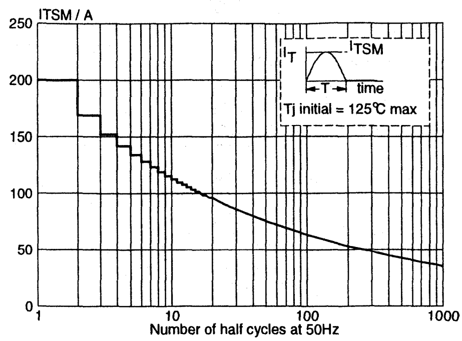


Fig.4. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

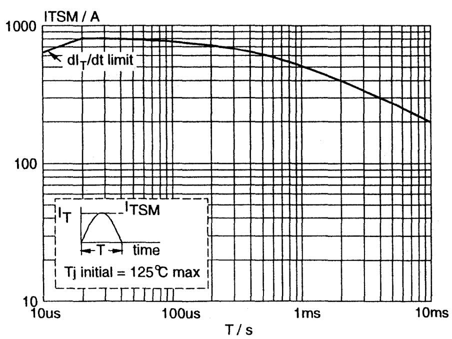


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq$ 10ms.

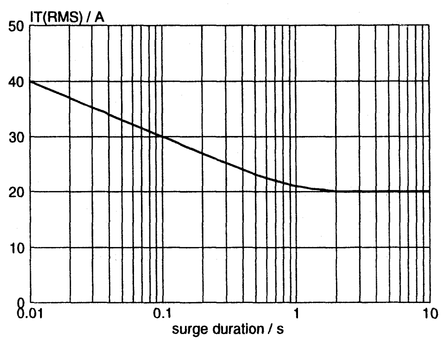


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq$ 103˚C.

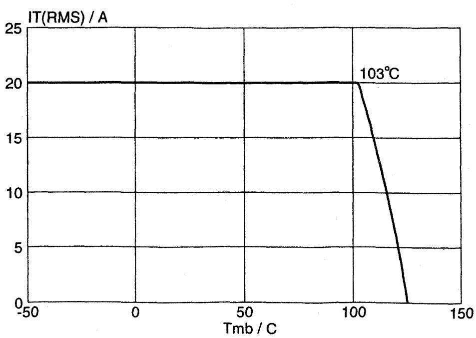


Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

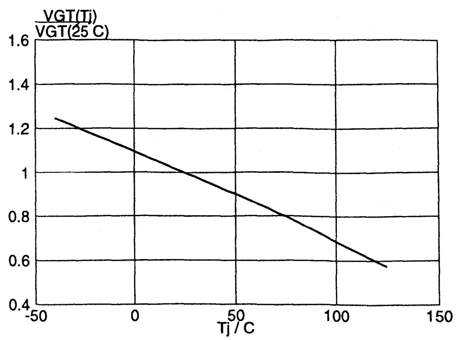


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)$/ V_{GT}(25˚C), versus junction temperature T_j.

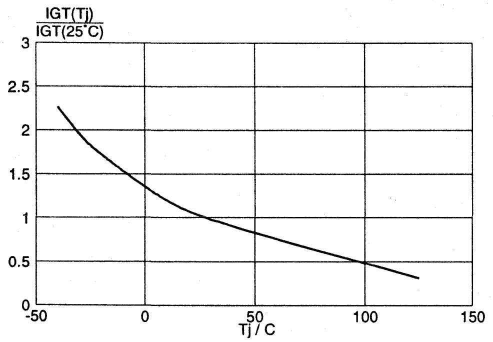


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

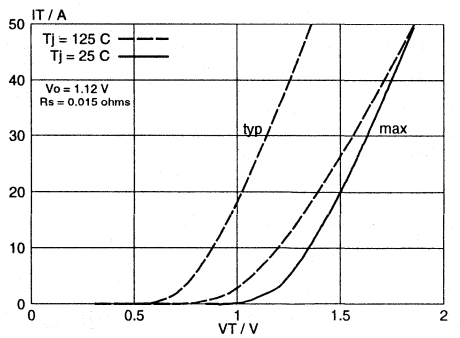


Fig.10. Typical and maximum on-state characteristic.

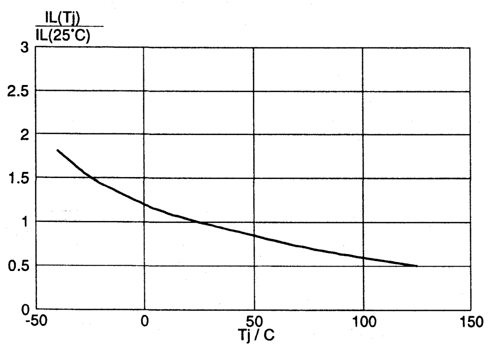


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.

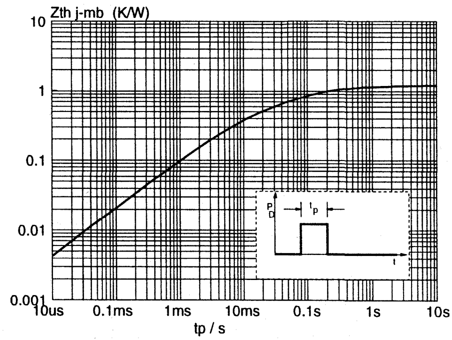


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width t_p.

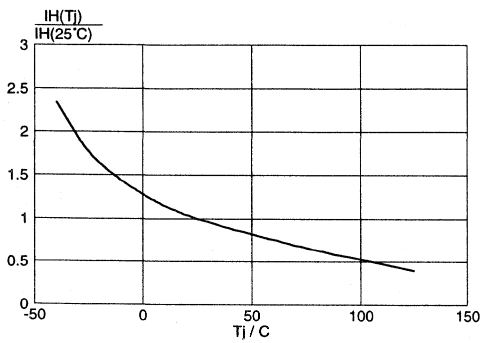


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j.

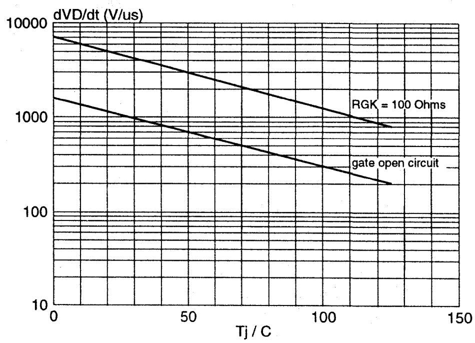


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

Thyristors logic level for RCD/ GFI/ LCCB applications

BT168 series

GENERAL DESCRIPTION

Glass passivated, sensitive gate thyristors in a plastic envelope, intended for use in Residual Current Devices/ Ground Fault Interrupters/ Leakage Current Circuit Breakers (RCD/ GFI/ LCCB) applications where a minimum I_{GT} limit is needed. These devices may be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

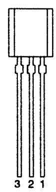
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	MAX.	UNIT
	BT168	B	D	E	G	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages	200	400	500	600	V
$I_{T(AV)}$	Average on-state current	0.5	0.5	0.5	0.5	A
$I_{T(RMS)}$	RMS on-state current	0.8	0.8	0.8	0.8	A
I_{TSM}	Non-repetitive peak on-state current	8	8	8	8	A

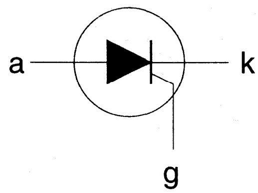
PINNING - TO92 variant

PIN	DESCRIPTION
1	anode
2	gate
3	cathode

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.				UNIT
				B	D	E	G	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages		-	200[1]	400[1]	500[1]	600[1]	V
$I_{T(AV)}$	Average on-state current	half sine wave; $T_{lead} \leq 83$ ˚C	-	0.5				A
$I_{T(RMS)}$	RMS on-state current	all conduction angles	-	0.8				A
I_{TSM}	Non-repetitive peak on-state current	half sine wave; T_j = 125 ˚C prior to surge; with reapplied $V_{DRM(max)}$ t = 10 ms	-	8				A
		t = 8.3 ms	-	9				A
I^2t	I^2t for fusing	t = 10 ms	-	0.32				A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	I_{TM} = 2 A; I_G = 10 mA; dI_G/dt = 100 mA/µs	-	50				A/µs
I_{GM}	Peak gate current		-	1				A
V_{GM}	Peak gate voltage		-	5				V
V_{RGM}	Peak reverse gate voltage		-	5				V
P_{GM}	Peak gate power		-	2				W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.1				W
T_{stg}	Storage temperature		-40	150				˚C
T_j	Operating junction temperature		-	125				˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}lead}$	Thermal resistance junction to lead		-	-	60	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	pcb mounted; lead length = 4mm	-	150	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 10 mA; gate open circuit	20	50	200	µA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.5 mA; R_{GK} = 1 kΩ	-	2	6	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.5 mA; R_{GK} = 1 kΩ	-	2	5	mA
V_T	On-state voltage	I_T = 1 A	-	1.2	1.35	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 10 mA; gate open circuit	-	0.5	0.8	V
		V_D = $V_{DRM(max)}$; I_T = 10 mA; T_j = 125 ˚C; gate open circuit	0.2	0.3	-	V
I_D, I_R	Off-state leakage current	V_D = $V_{DRM(max)}$; V_R = $V_{RRM(max)}$; T_j = 125 ˚C; R_{GK} = 1 kΩ	-	0.05	0.1	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; R_{GK} = 1 kΩ	-	25	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 2 A; V_D = $V_{DRM(max)}$; I_G = 10 mA; dI_G/dt = 0.1 A/µs	-	2	-	µs
t_q	Circuit commutated turn-off time	V_D = 67% $V_{DRM(max)}$; T_j = 125 ˚C; I_{TM} = 1.6 A; V_R = 35 V; dI_{TM}/dt = 30 A/µs; dV_D/dt = 2 V/µs; R_{GK} = 1 kΩ	-	100	-	µs

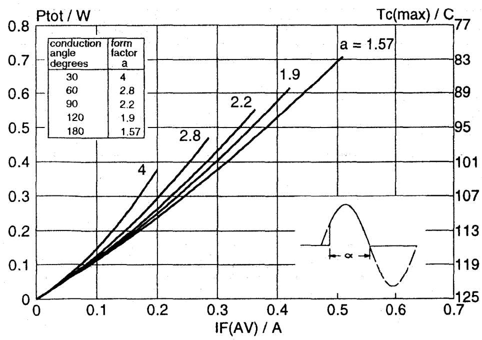


Fig.1. Maximum on-state dissipation, P_{tot}, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}$/ $I_{T(AV)}$.

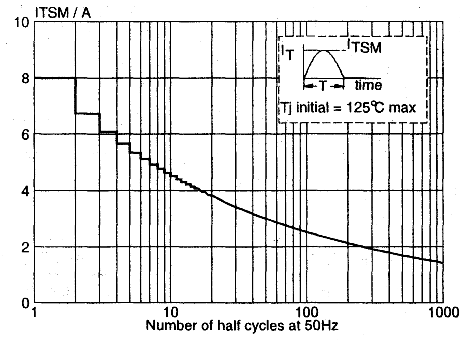


Fig.4. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

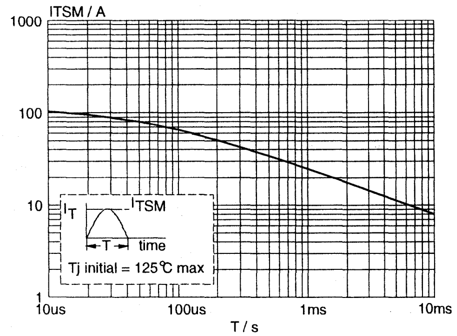


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq$ 10ms.

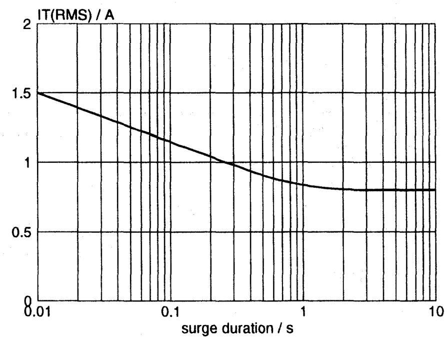


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{lead} \leq$ 83˚C.

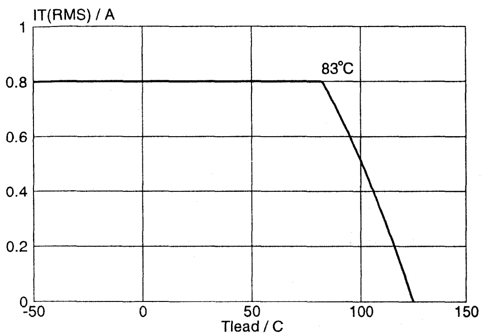


Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus lead temperature, T_{lead}.

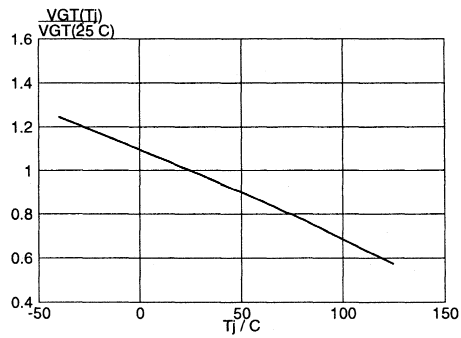


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)$/ V_{GT}(25˚C), versus junction temperature T_j.

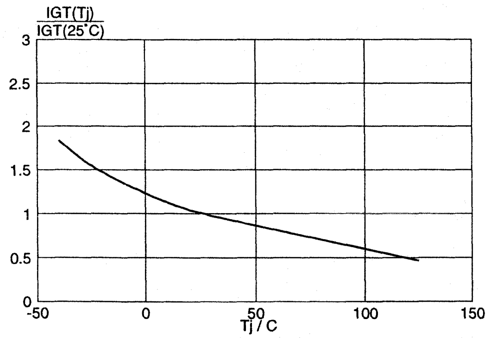


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature T_j.

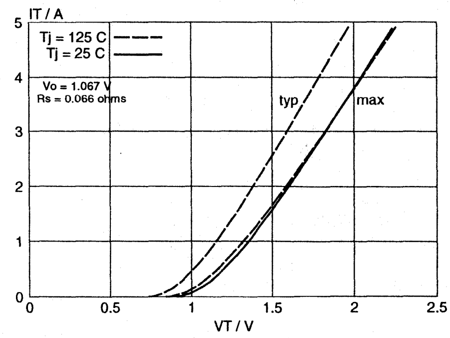


Fig.10. Typical and maximum on-state characteristic.

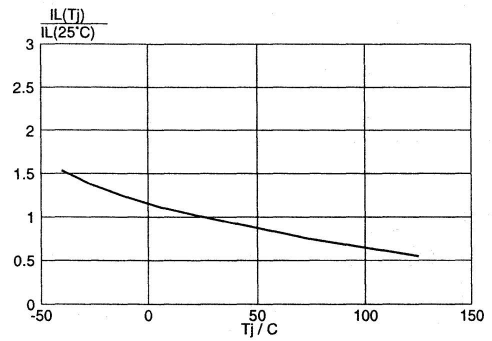


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature T_j, R_{GK} = 1 kΩ.

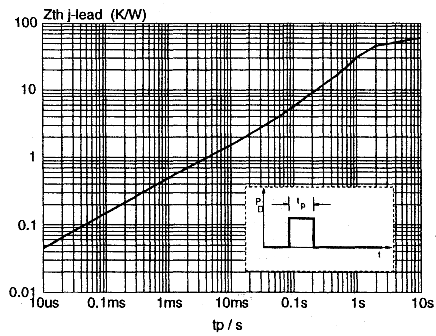


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}lead}$, versus pulse width t_p.

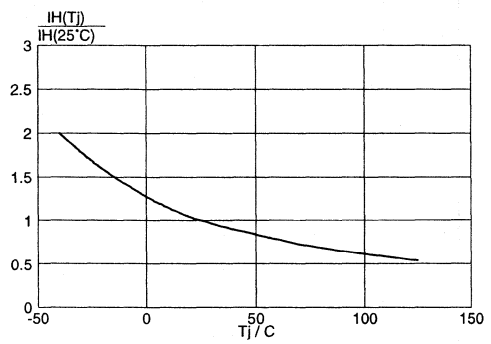


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature T_j, R_{GK} = 1 kΩ.

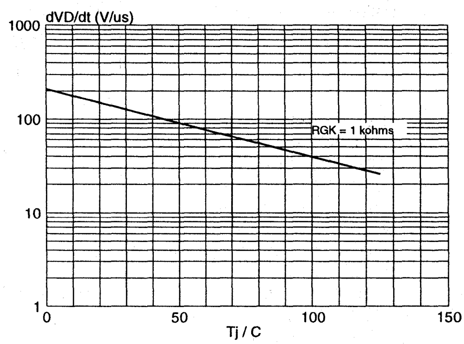


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

Thyristors
logic level for RCD/ GFI/ LCCB applications

BT168W series

GENERAL DESCRIPTION

Glass passivated, sensitive gate thyristors in a plastic envelope suitable for surface mounting, intended for use in Residual Current Devices/ Ground Fault Interrupters/ Leakage Current Circuit Breakers (RCD/ GFI/ LCCB) applications where a minimum I_{GT} limit is needed. These devices may be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

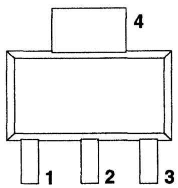
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	MAX.	UNIT
	BT168	BW	DW	EW	GW	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages	200	400	500	600	V
$I_{T(AV)}$	Average on-state current	0.6	0.6	0.6	0.6	A
$I_{T(RMS)}$	RMS on-state current	1	1	1	1	A
I_{TSM}	Non-repetitive peak on-state current	8	8	8	8	A

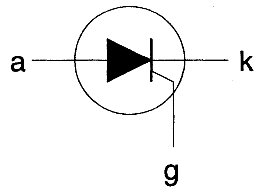
PINNING - SOT223

PIN	DESCRIPTION
1	cathode
2	anode
3	gate
tab	anode

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.				UNIT
				B	D	E	G	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages		-	200[1]	400[1]	500[1]	600[1]	V
$I_{T(AV)}$	Average on-state current	half sine wave; $T_{sp} \leq 112$ ˚C	-	0.63				A
$I_{T(RMS)}$	RMS on-state current	all conduction angles	-	1				A
I_{TSM}	Non-repetitive peak on-state current	t = 10 ms	-	8				A
		t = 8.3 ms	-	9				A
		half sine wave; T_j = 125 ˚C prior to surge; with reapplied $V_{DRM(max)}$						
I^2t	I^2t for fusing	t = 10 ms	-	0.32				A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	I_{TM} = 2 A; I_G = 10 mA; dI_G/dt = 100 mA/μs	-	50				A/μs
I_{GM}	Peak gate current		-	1				A
V_{GM}	Peak gate voltage		-	5				V
V_{RGM}	Peak reverse gate voltage		-	5				V
P_{GM}	Peak gate power		-	2				W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.1				W
T_{stg}	Storage temperature		-40	150				˚C
T_j	Operating junction temperature		-	125				˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/μs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}sp}$	Thermal resistance junction to solder point		-	-	15	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	pcb mounted, minimum footprint	-	156	-	K/W
		pcb mounted, pad area as in fig:14	-	70	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 10 mA; gate open circuit	20	50	200	μA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.5 mA; R_{GK} = 1 kΩ	-	2	6	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.5 mA; R_{GK} = 1 kΩ	-	2	5	mA
V_T	On-state voltage	I_T = 2 A	-	1.35	1.5	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 10 mA; gate open circuit	-	0.5	0.8	V
		$V_D = V_{DRM(max)}$; I_T = 10 mA; T_j = 125 ˚C; gate open circuit	0.2	0.3	-	V
I_D, I_R	Off-state leakage current	$V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; T_j = 125 ˚C; R_{GK} = 1 kΩ	-	0.05	0.1	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; R_{GK} = 1 kΩ	-	25	-	V/μs
t_{gt}	Gate controlled turn-on time	I_{TM} = 2 A; $V_D = V_{DRM(max)}$; I_G = 10 mA; dI_G/dt = 0.1 A/μs	-	2	-	μs
t_q	Circuit commutated turn-off time	V_D = 67% $V_{DRM(max)}$; T_j = 125 ˚C; I_{TM} = 1.6 A; V_R = 35 V; dI_{TM}/dt = 30 A/μs; dV_D/dt = 2 V/μs; R_{GK} = 1 kΩ	-	100	-	μs

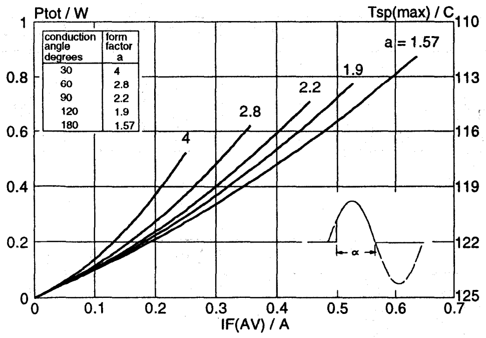


Fig.1. Maximum on-state dissipation, P_{tot}, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}$/ $I_{T(AV)}$.

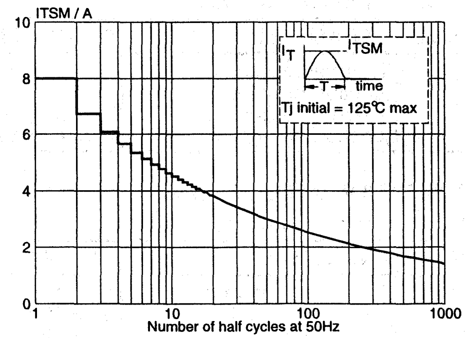


Fig.4. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

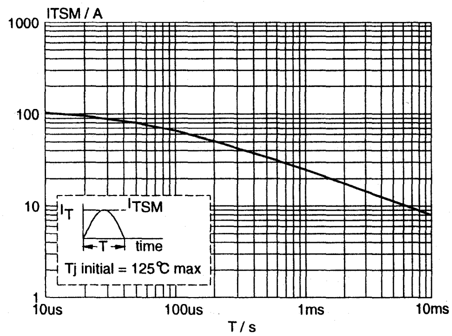


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq$ 10ms.

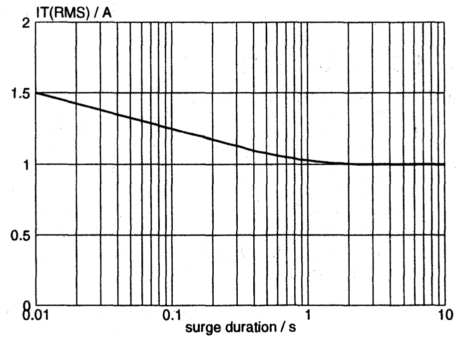


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{sp} \leq$ 112˚C.

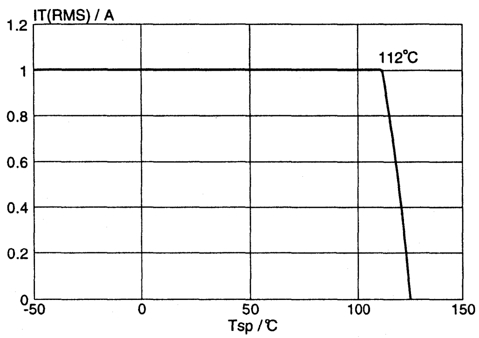


Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus solder point temperature T_{sp}.

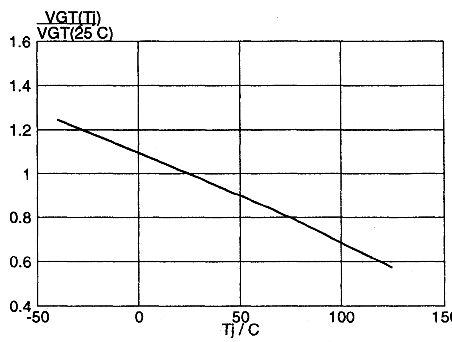


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)$/ V_{GT}(25˚C), versus junction temperature T_j.

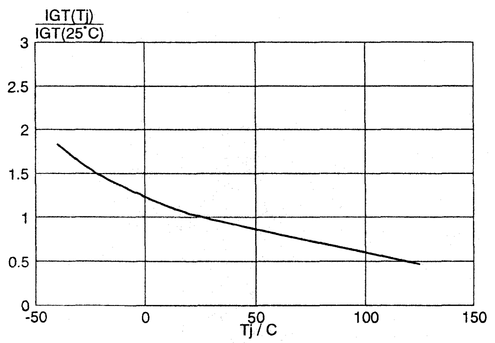


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25^\circ C)$, versus junction temperature T_j.

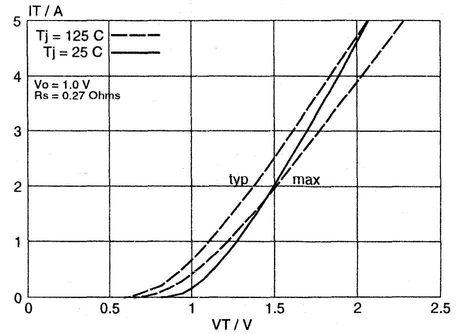


Fig.10. Typical and maximum on-state characteristic.

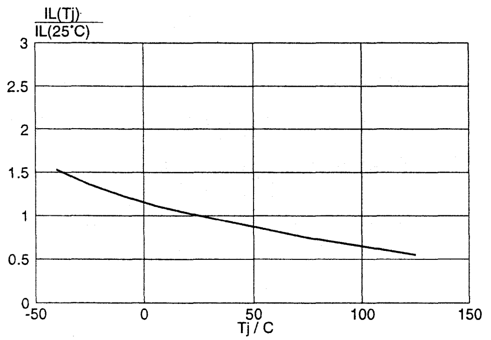


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25^\circ C)$, versus junction temperature T_j, $R_{GK} = 1\ k\Omega$.

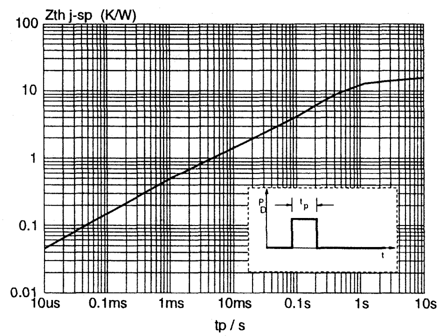


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}sp}$, versus pulse width t_p.

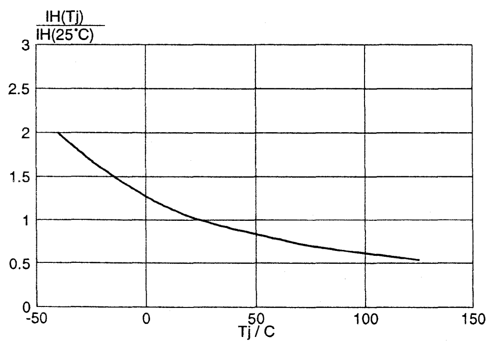


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25^\circ C)$, versus junction temperature T_j, $R_{GK} = 1\ k\Omega$.

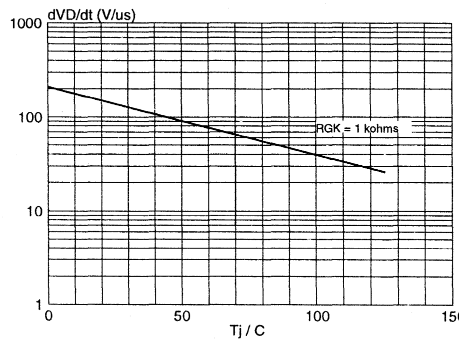


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

MOUNTING INSTRUCTIONS

Dimensions in mm.

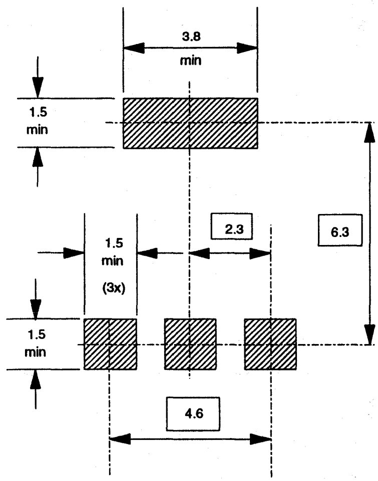


Fig.13. soldering pattern for surface mounting SOT223.

PRINTED CIRCUIT BOARD

Dimensions in mm.

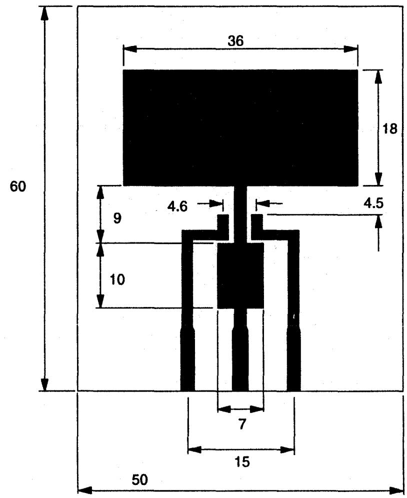


Fig.14. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).

GENERAL DESCRIPTION

Glass passivated, sensitive gate thyristors in a plastic envelope, intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

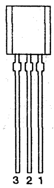
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	MAX.	UNIT
	BT169	B	D	E	G	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages	200	400	500	600	V
$I_{T(AV)}$	Average on-state current	0.5	0.5	0.5	0.5	A
$I_{T(RMS)}$	RMS on-state current	0.8	0.8	0.8	0.8	A
I_{TSM}	Non-repetitive peak on-state current	8	8	8	8	A

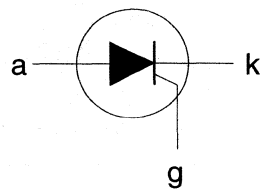
PINNING - TO92 variant

PIN	DESCRIPTION
1	anode
2	gate
3	cathode

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.				UNIT
				B	D	E	G	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages		-	200[1]	400[1]	500[1]	600[1]	V
$I_{T(AV)}$	Average on-state current	half sine wave; $T_{lead} \leq 83$ ˚C	-	0.5				A
$I_{T(RMS)}$	RMS on-state current	all conduction angles	-	0.8				A
I_{TSM}	Non-repetitive peak on-state current	t = 10 ms	-	8				A
		t = 8.3 ms half sine wave; T_j = 125 ˚C prior to surge; with reapplied $V_{DRM(max)}$	-	9				A
I^2t	I^2t for fusing	t = 10 ms	-	0.32				A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	I_{TM} = 2 A; I_G = 10 mA; dI_G/dt = 100 mA/µs	-	50				A/µs
I_{GM}	Peak gate current		-	1				A
V_{GM}	Peak gate voltage		-	5				V
V_{RGM}	Peak reverse gate voltage		-	5				V
P_{GM}	Peak gate power		-	2				W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.1				W
T_{stg}	Storage temperature		-40	150				˚C
T_j	Operating junction temperature		-	125				˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}lead}$	Thermal resistance junction to lead		-	-	60	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	pcb mounted; lead length = 4mm	-	150	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 10 mA; gate open circuit	-	50	200	µA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.5 mA; R_{GK} = 1 kΩ	-	2	6	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.5 mA; R_{GK} = 1 kΩ	-	2	5	mA
V_T	On-state voltage	I_T = 1 A	-	1.2	1.35	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 10 mA; gate open circuit	-	0.5	0.8	V
		$V_D = V_{DRM(max)}$; I_T = 10 mA; T_j = 125 ˚C; gate open circuit	0.2	0.3	-	V
I_D, I_R	Off-state leakage current	$V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; T_j = 125 ˚C; R_{GK} = 1 kΩ	-	0.05	0.1	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; R_{GK} = 1 kΩ	-	25	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 2 A; $V_D = V_{DRM(max)}$; I_G = 10 mA; dI_G/dt = 0.1 A/µs	-	2	-	µs
t_q	Circuit commutated turn-off time	V_D = 67% $V_{DRM(max)}$; T_j = 125 ˚C; I_{TM} = 1.6 A; V_R = 35 V; dI_{TM}/dt = 30 A/µs; dV_D/dt = 2 V/µs; R_{GK} = 1 kΩ	-	100	-	µs

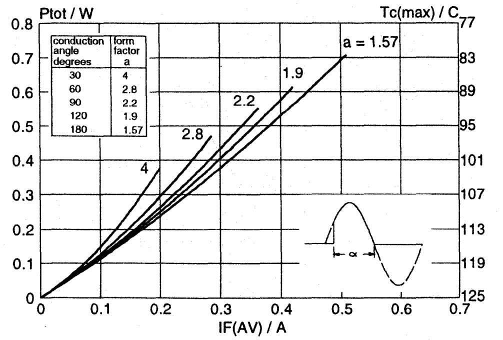


Fig.1. Maximum on-state dissipation, P_{tot}, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}/I_{T(AV)}$.

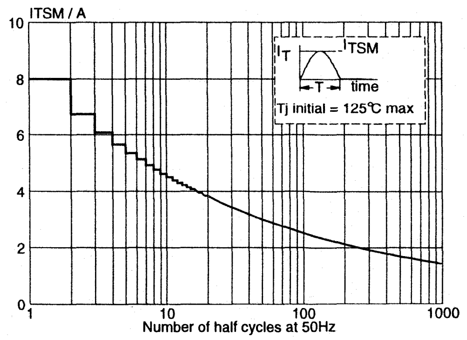


Fig.4. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

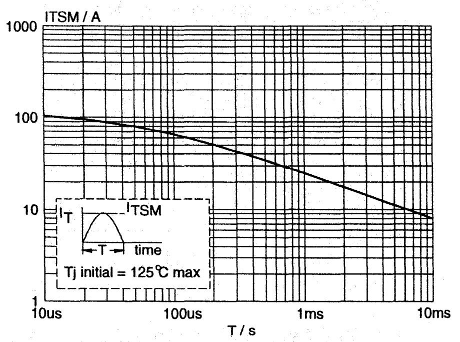


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq$ 10ms.

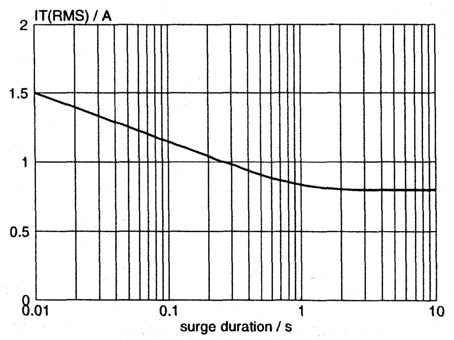


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{lead} \leq$ 83˚C.

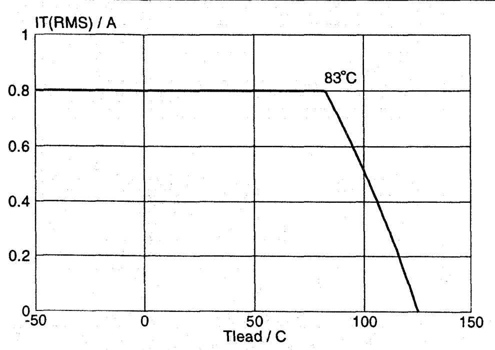


Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus lead temperature, T_{lead}.

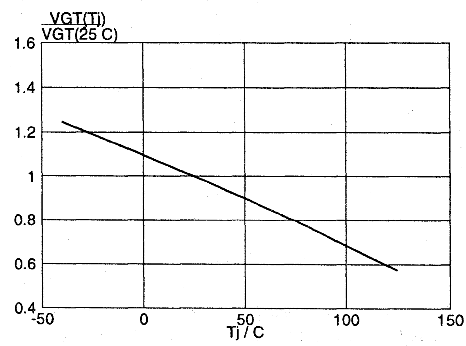


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25˚C)$, versus junction temperature T_j.

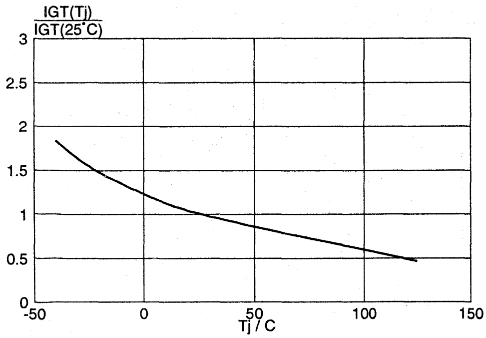


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/I_{GT}(25˚C)$, versus junction temperature T_j.

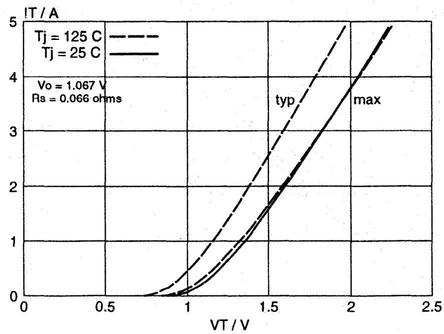


Fig.10. Typical and maximum on-state characteristic.

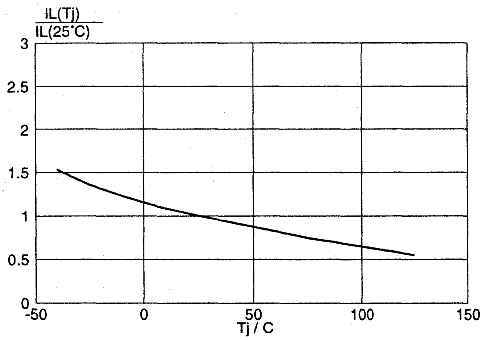


Fig.8. Normalised latching current $I_L(T_j)/I_L(25˚C)$, versus junction temperature T_j, $R_{GK} = 1\ k\Omega$.

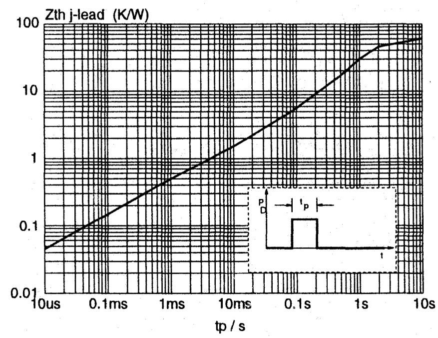


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}lead}$, versus pulse width t_p.

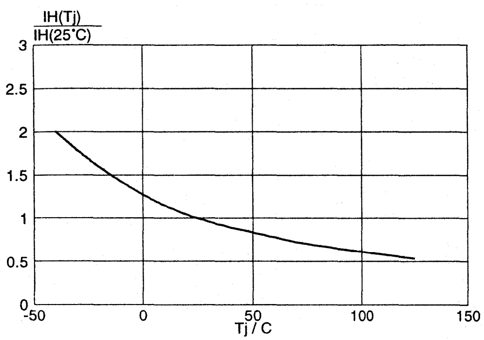


Fig.9. Normalised holding current $I_H(T_j)/I_H(25˚C)$, versus junction temperature T_j, $R_{GK} = 1\ k\Omega$.

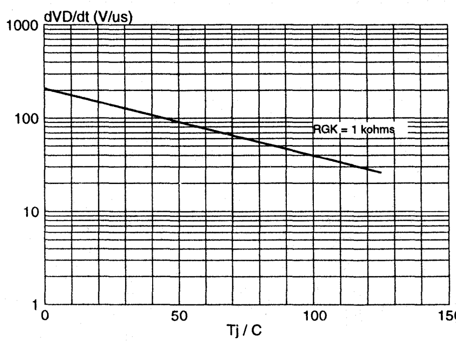


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

Thyristor logic level

BT169DW

GENERAL DESCRIPTION

Glass passivated, sensitive gate thyristor in a plastic envelope, suitable for surface mounting, intended for use in general purpose switching and phase control applications. This device is intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

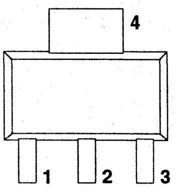
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages	400	V
$I_{T(AV)}$	Average on-state current	0.6	A
$I_{T(RMS)}$	RMS on-state current	1	A
I_{TSM}	Non-repetitive peak on-state current	8	A

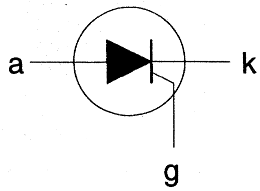
PINNING - SOT223

PIN	DESCRIPTION
1	cathode
2	anode
3	gate
tab	anode

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages		-	400[1]	V
$I_{T(AV)}$	Average on-state current	half sine wave; $T_{sp} \leq 112$ ˚C	-	0.63	A
$I_{T(RMS)}$	RMS on-state current	all conduction angles	-	1	A
I_{TSM}	Non-repetitive peak on-state current	half sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$			
		t = 10 ms	-	8	A
		t = 8.3 ms	-	9	A
I^2t	I^2t for fusing	t = 10 ms	-	0.32	A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 2$ A; $I_G = 10$ mA; $dI_G/dt = 100$ mA/µs	-	50	A/µs
I_{GM}	Peak gate current		-	1	A
V_{GM}	Peak gate voltage		-	5	V
V_{RGM}	Peak reverse gate voltage		-	5	V
P_{GM}	Peak gate power		-	2	W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.1	W
T_{stg}	Storage temperature		-40	150	˚C
T_j	Operating junction temperature		-	125	˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-sp}$	Thermal resistance junction to solder point		-	-	15	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	pcb mounted, minimum footprint	-	156	-	K/W
		pcb mounted; pad area as in fig:14	-	70	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 10 mA; gate open circuit	-	50	200	µA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.5 mA; R_{GK} = 1 kΩ	-	2	6	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.5 mA; R_{GK} = 1 kΩ	-	2	5	mA
V_T	On-state voltage	I_T = 2 A	-	1.35	1.5	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 10 mA; gate open circuit	-	0.5	0.8	V
		V_D = $V_{DRM(max)}$; I_T = 10 mA; T_j = 125 ˚C; gate open circuit	0.2	0.3	-	V
I_D, I_R	Off-state leakage current	V_D = $V_{DRM(max)}$; V_R = $V_{RRM(max)}$; T_j = 125 ˚C; R_{GK} = 1 kΩ	-	0.05	0.1	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} =67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; R_{GK} = 1k Ω	-	25	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 2 A; V_D = $V_{DRM(max)}$; I_G = 10 mA; dI_G/dt = 0.1 A/µs	-	2	-	µs
t_q	Circuit commutated turn-off time	V_D = 67% $V_{DRM(max)}$; T_j = 125 ˚C; I_{TM} = 1.6 A; V_R = 35 V; dI_{TM}/dt = 30 A/µs; dV_D/dt = 2 V/µs; R_{GK} = 1 kΩ	-	100	-	µs

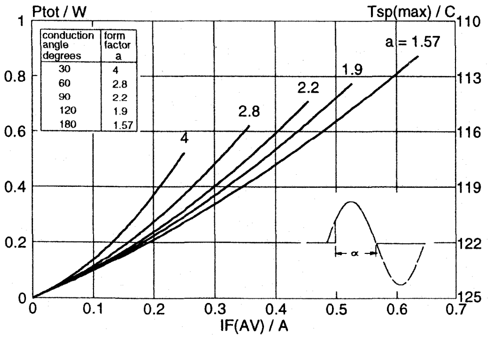


Fig.1. Maximum on-state dissipation, P_{tot}, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}/I_{T(AV)}$.

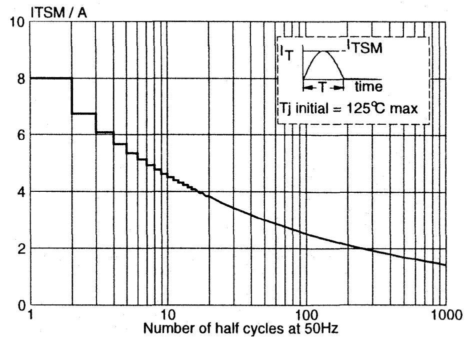


Fig.4. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

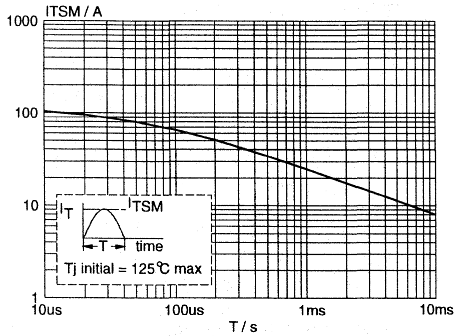


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq$ 10ms.

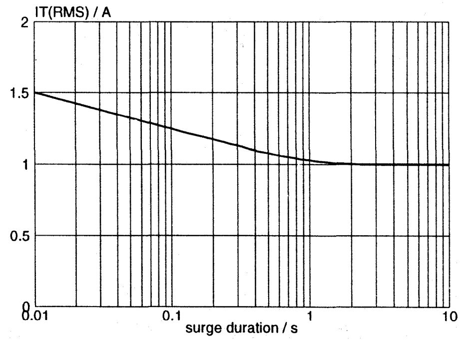


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{sp} \leq$ 112˚C.

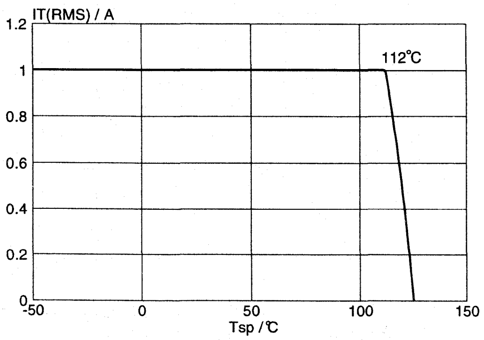


Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus solder point temperature T_{sp}.

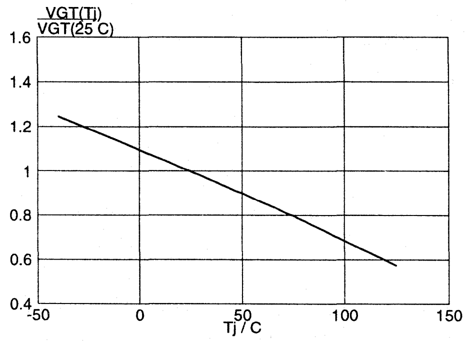


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25˚C)$, versus junction temperature T_j.

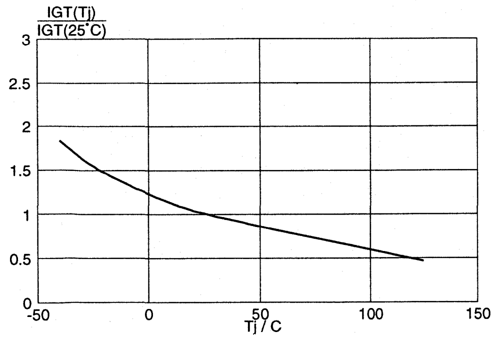


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

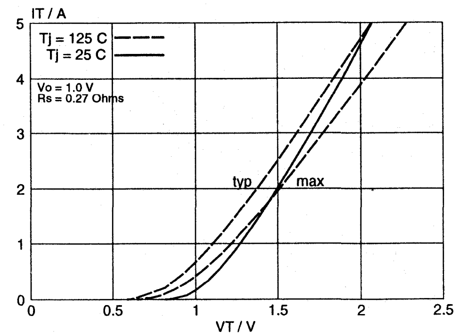


Fig.10. Typical and maximum on-state characteristic.

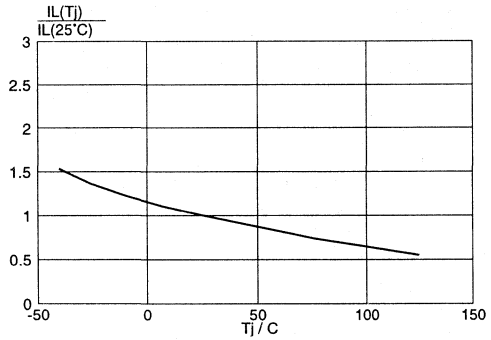


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j, R_{GK} = 1 kΩ.

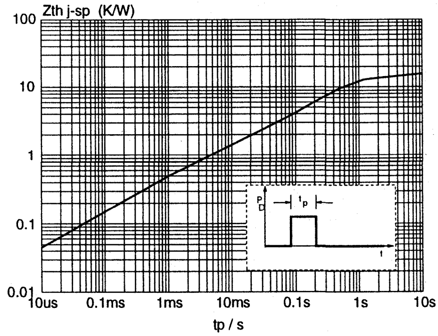


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}sp}$, versus pulse width t_p.

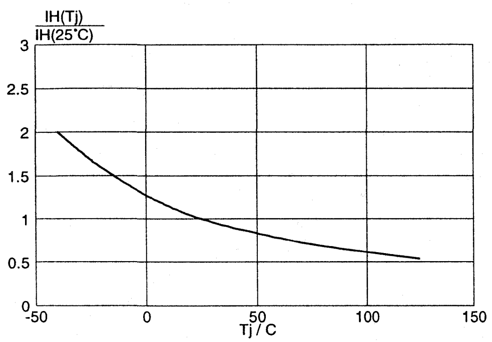


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j, R_{GK} = 1 kΩ.

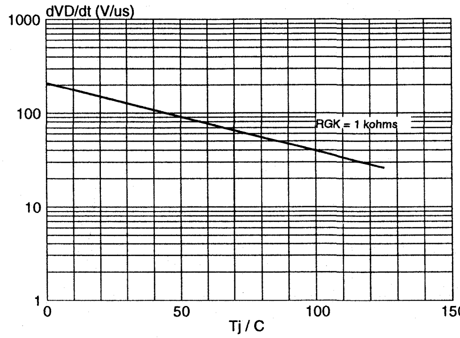


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

MOUNTING INSTRUCTIONS

Dimensions in mm.

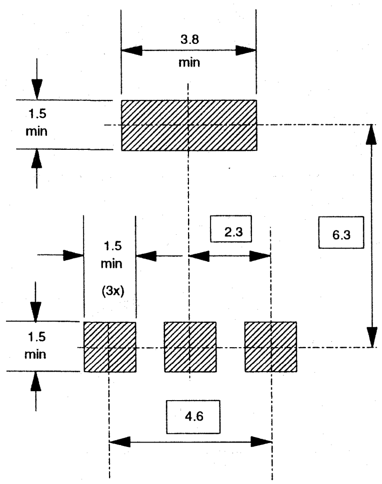


Fig.13. soldering pattern for surface mounting SOT223.

PRINTED CIRCUIT BOARD

Dimensions in mm.

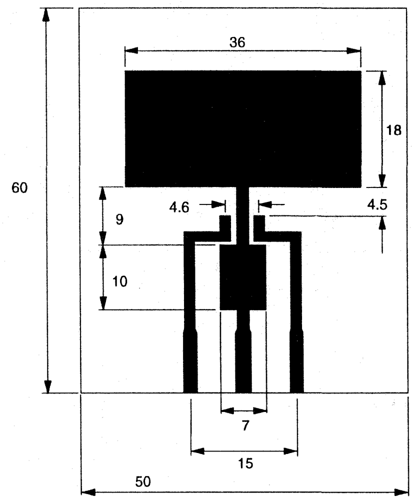


Fig.14. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 µm thick).

Thyristors logic level

BT258 series

GENERAL DESCRIPTION

Glass passivated, sensitive gate thyristors in a plastic envelope, intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

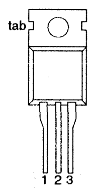
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT258-	**500R**	**600R**	**800R**	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(AV)}$	Average on-state current	5	5	5	A
$I_{T(RMS)}$	RMS on-state current	8	8	8	A
I_{TSM}	Non-repetitive peak on-state current	65	65	65	A

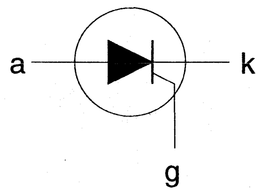
PINNING - TO220AB

PIN	DESCRIPTION
1	cathode
2	anode
3	gate
tab	anode

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500R	-600R	-800R	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(AV)}$	Average on-state current	half sine wave; $T_{mb} \leq 111$ ˚C	-	5			A
$I_{T(RMS)}$	RMS on-state current	all conduction angles	-	8			A
I_{TSM}	Non-repetitive peak on-state current	half sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 10 ms	-	65			A
		t = 8.3 ms	-	71			A
I^2t	I^2t for fusing	t = 10 ms	-	21			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 10$ A; $I_G = 50$ mA; $dI_G/dt = 50$ mA/μs	-	50			A/μs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
V_{RGM}	Peak reverse gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/μs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base		-	-	2.0	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A	-	50	200	µA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A	-	0.4	10	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	0.3	6	mA
V_T	On-state voltage	I_T = 16 A	-	1.3	1.5	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.4	1.5	V
		V_D = $V_{DRM(max)}$; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.3	-	V
I_D, I_R	Off-state leakage current	V_D = $V_{DRM(max)}$; V_R = $V_{RRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; R_{GK} = 100 Ω	50	100	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 10 A; V_D = $V_{DRM(max)}$; I_G = 5 mA; dI_G/dt = 0.2 A/µs	-	2	-	µs
t_q	Circuit commutated turn-off time	V_D = 67% $V_{DRM(max)}$; T_j = 125 ˚C; I_{TM} = 12 A; V_R = 24 V; dI_{TM}/dt = 10 A/µs; dV_D/dt = 2 V/µs; R_{GK} = 1 kΩ	-	100	-	µs

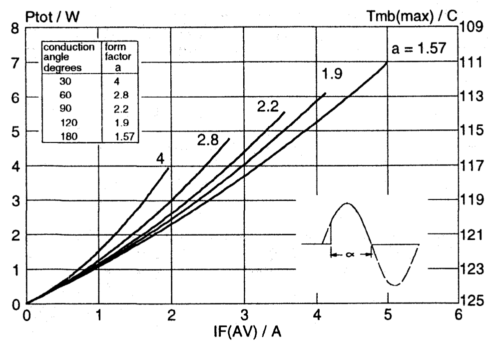


Fig.1. Maximum on-state dissipation, P_{tot}, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}$/ $I_{T(AV)}$.

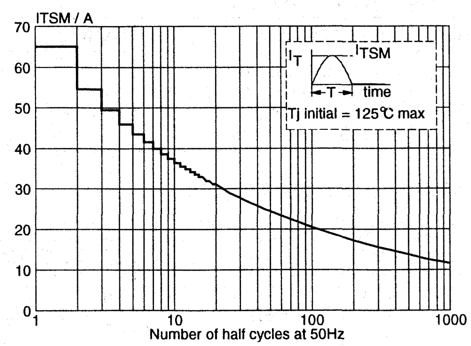


Fig.4. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

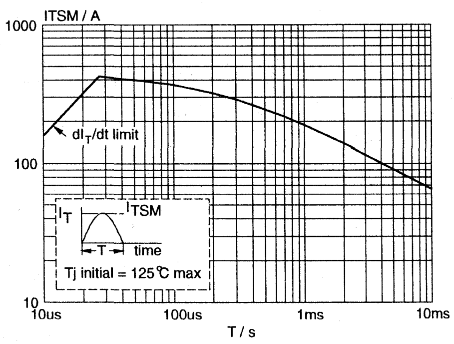


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq$ 10ms.

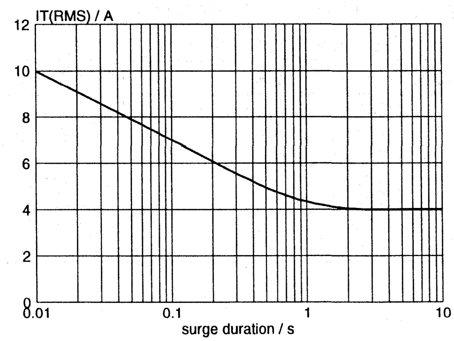


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq$ 111˚C.

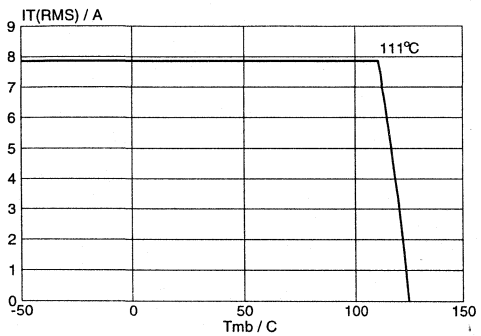


Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

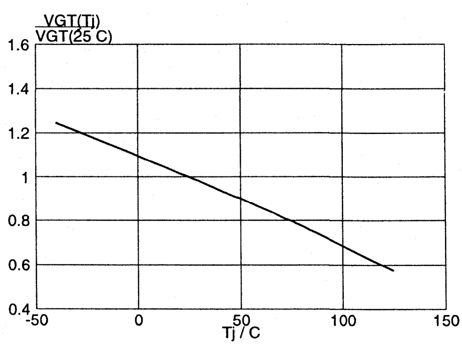


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)$/ V_{GT}(25˚C), versus junction temperature T_j.

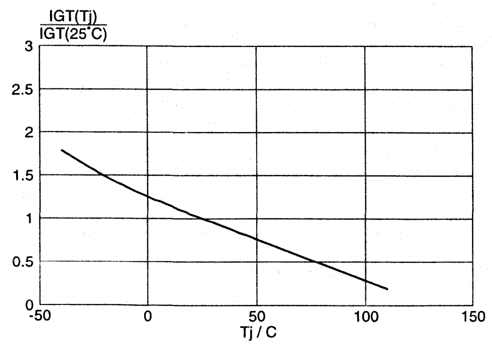


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

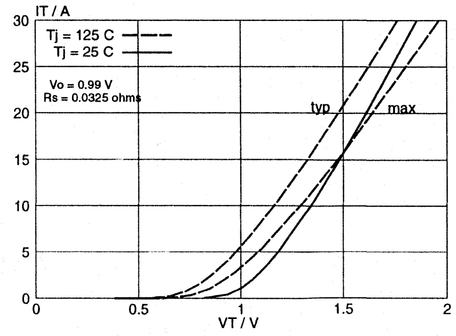


Fig.10. Typical and maximum on-state characteristic.

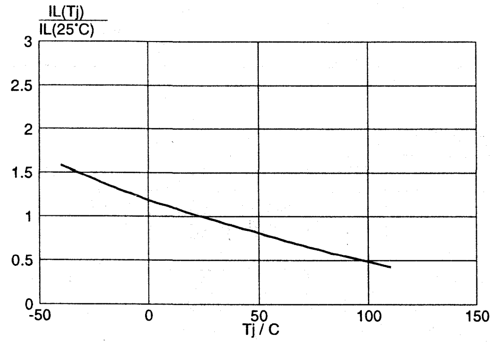


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.

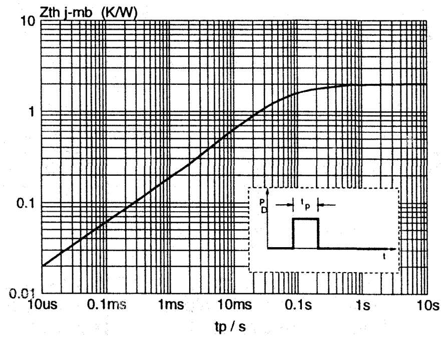


Fig.11. Transient thermal impedance $Z_{th\,j\text{-}mb}$, versus pulse width t_p.

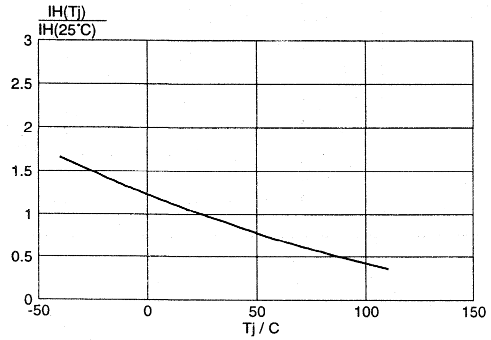


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j.

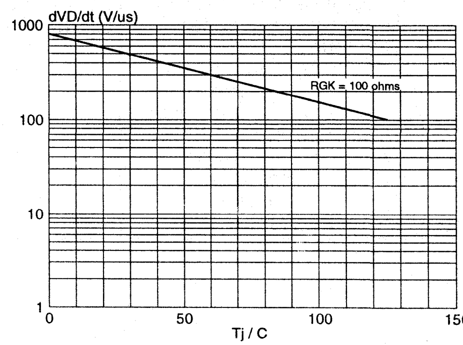


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

Thyristors — BT300 series

GENERAL DESCRIPTION

Glass passivated thyristors in a plastic envelope, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

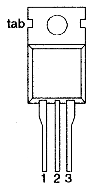
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT300-	500R	600R	800R	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(AV)}$	Average on-state current	5	5	5	A
$I_{T(RMS)}$	RMS on-state current	8	8	8	A
I_{TSM}	Non-repetitive peak on-state current	65	65	65	A

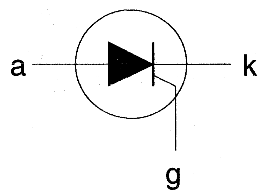
PINNING - TO220AB

PIN	DESCRIPTION
1	cathode
2	anode
3	gate
tab	anode

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500R	-600R	-800R	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(AV)}$	Average on-state current	half sine wave; $T_{mb} \leq 111$ ˚C	-	5			A
$I_{T(RMS)}$	RMS on-state current	all conduction angles	-	8			A
I_{TSM}	Non-repetitive peak on-state current	half sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 10 ms	-	65			A
		t = 8.3 ms	-	71			A
I^2t	I^2t for fusing	t = 10 ms	-	21			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 10$ A; $I_G = 50$ mA; $dI_G/dt = 50$ mA/µs	-	50			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
V_{RGM}	Peak reverse gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A	-	2	15	µA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A	-	10	40	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	10	20	mA
V_T	On-state voltage	I_T = 16 A	-	1.3	1.5	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.6	1.5	V
		$V_D = V_{DRM(max)}$; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D, I_R	Off-state leakage current	$V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform.				
		Gate open circuit	50	100	-	V/µs
		R_{GK} = 100 Ω	200	1000	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 10 A; $V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs
t_q	Circuit commutated turn-off time	V_D = 67% $V_{DRM(max)}$; T_j = 125 ˚C; I_{TM} = 12 A; V_R = 25 V; dI_{TM}/dt = 30 A/µs; dV_D/dt = 50 V/µs; R_{GK} = 100 Ω	-	70	-	µs

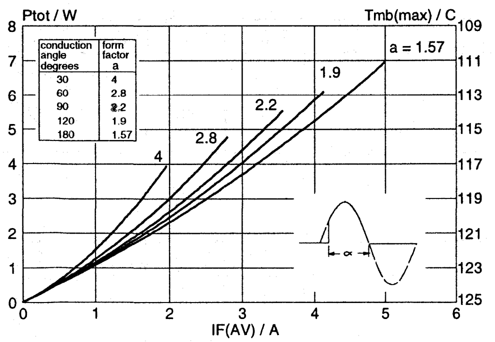


Fig.1. Maximum on-state dissipation, P_{tot}, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}$/ $I_{T(AV)}$.

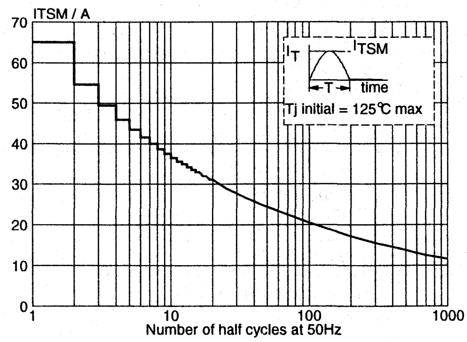


Fig.4. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

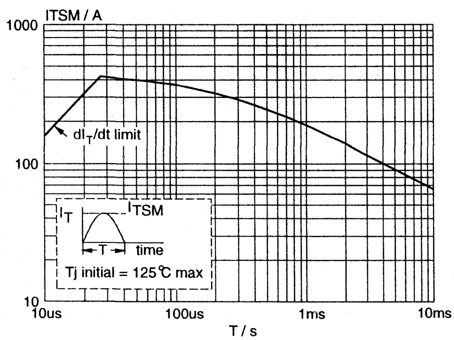


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq$ 10ms.

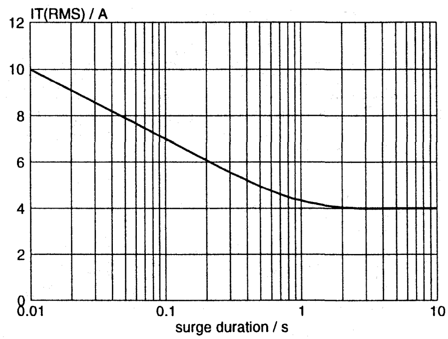


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq$ 111˚C.

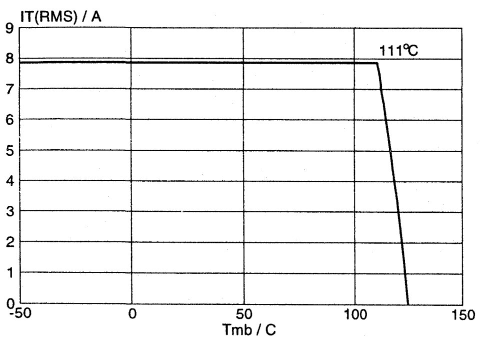


Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

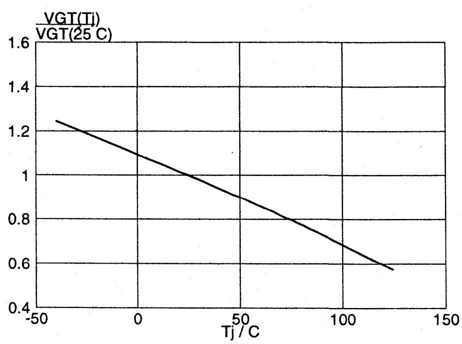


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)$/ V_{GT}(25˚C), versus junction temperature T_j.

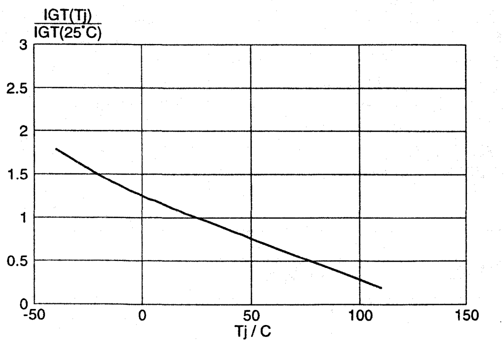


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

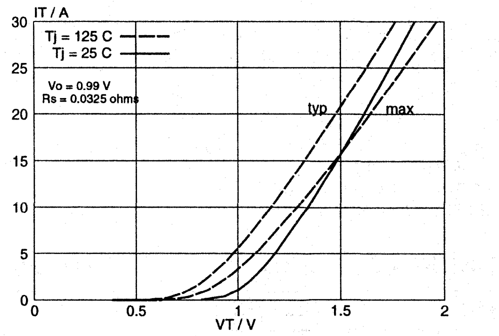


Fig.10. Typical and maximum on-state characteristic.

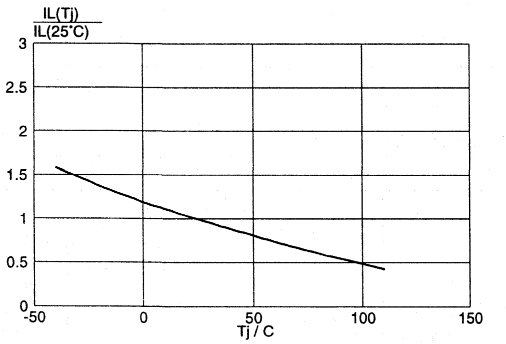


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.

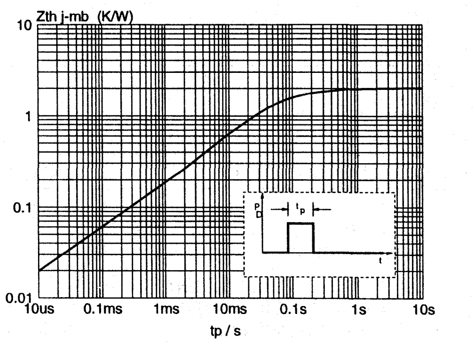


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width t_p.

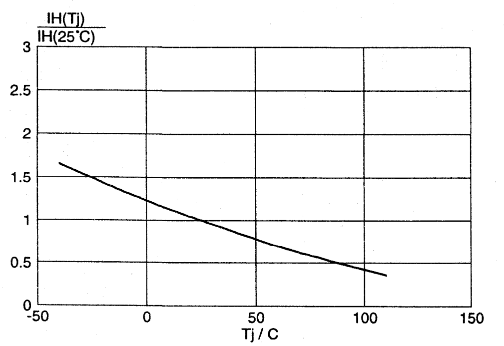


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j.

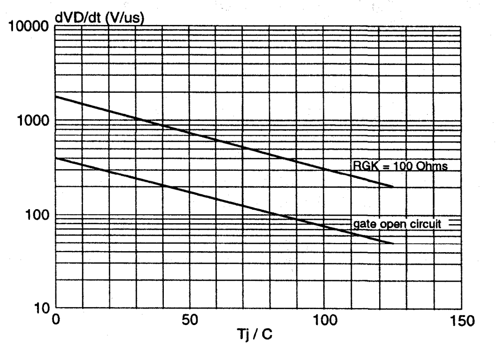


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

GENERAL DESCRIPTION

Glass passivated triacs in a plastic envelope, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

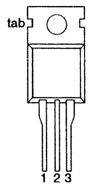
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BTA140-	**500**	**600**	**800**	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	25	25	25	A
I_{TSM}	Non-repetitive peak on-state current	180	180	180	A

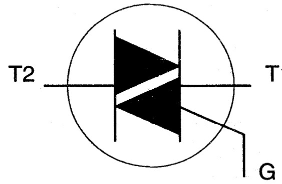
PINNING - TO220AB

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
tab	main terminal 2

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	**-600**	**-800**	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 91$ ˚C	-	25			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 20 ms	-	180			A
		t = 16.7 ms	-	200			A
I^2t	I^2t for fusing	t = 10 ms	-	160			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 30$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs					
		T2+ G+	-	50			A/µs
		T2+ G-	-	50			A/µs
		T2- G-	-	50			A/µs
		T2- G+	-	10			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	full cycle	-	-	1.0	K/W
		half cycle	-	-	1.4	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	-	6	35	mA
		T2+ G-	-	10	35	mA
		T2- G-	-	11	35	mA
		T2- G+	-	23	70	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	8	40	mA
		T2+ G-	-	30	60	mA
		T2- G-	-	18	40	mA
		T2- G+	-	15	60	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+	-	7	30	mA
		T2-	-	12	30	mA
V_T	On-state voltage	I_T = 30 A	-	1.2	1.55	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	$V_D = V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	100	300	-	V/μs
dV_{com}/dt	Critical rate of change of commutating voltage	V_{DM} = 400 V; T_j = 95 ˚C; $I_{T(RMS)}$ = 25 A; dI_{com}/dt = 9 A/ms; gate open circuit	-	10	-	V/μs
t_{gt}	Gate controlled turn-on time	I_{TM} = 30 A; $V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/μs	-	2	-	μs

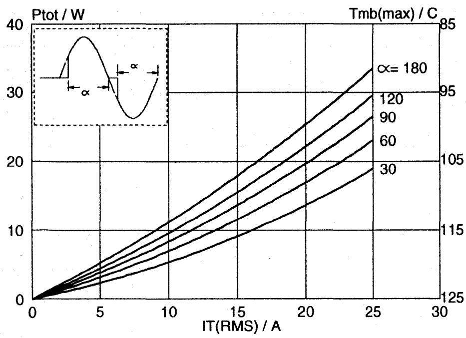


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

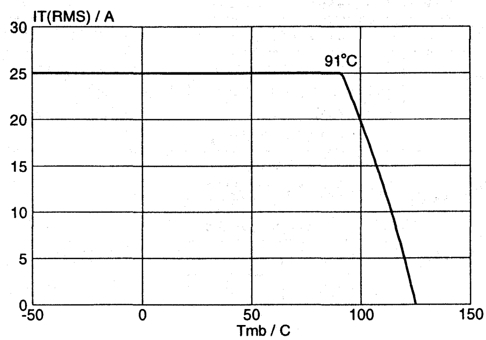


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

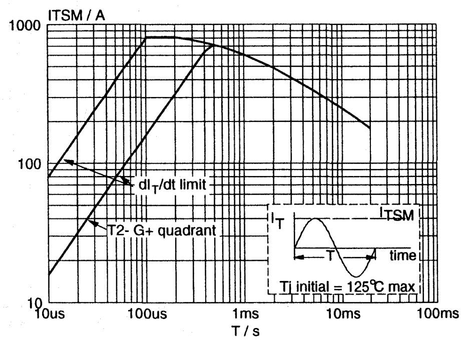


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq$ 20ms.

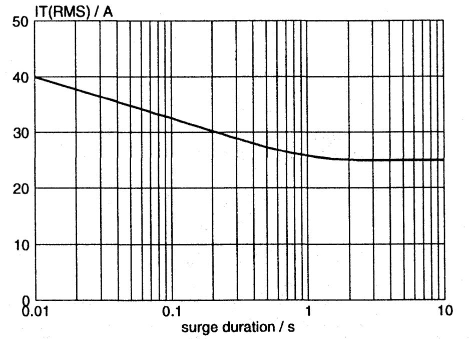


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq$ 91˚C.

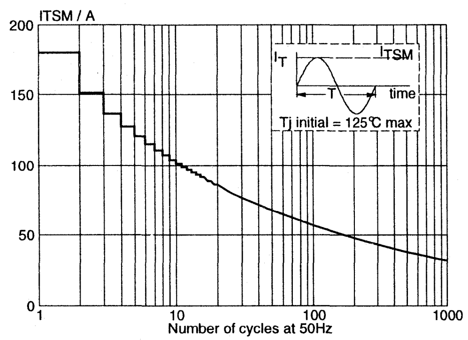


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

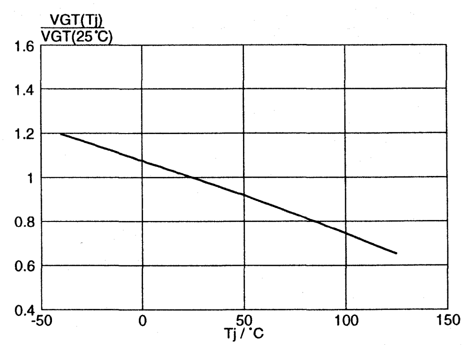


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)$/ V_{GT}(25˚C), versus junction temperature T_j.

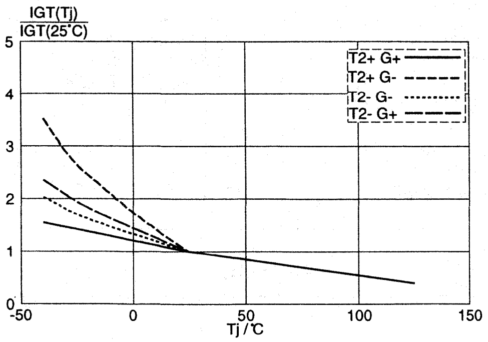


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/\ I_{GT}(25˚C)$, versus junction temperature T_j.

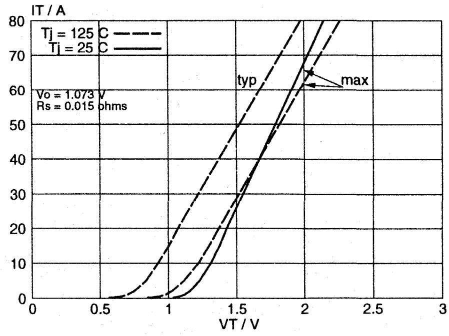


Fig.10. Typical and maximum on-state characteristic.

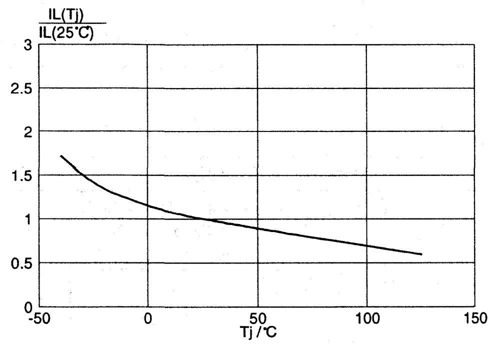


Fig.8. Normalised latching current $I_L(T_j)/\ I_L(25˚C)$, versus junction temperature T_j.

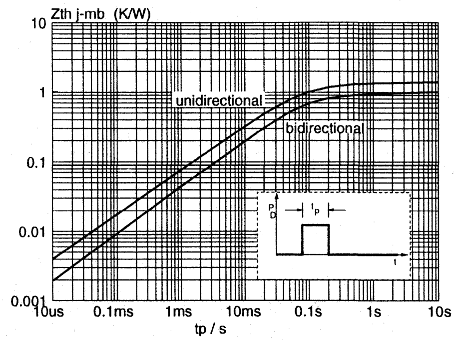


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width t_p.

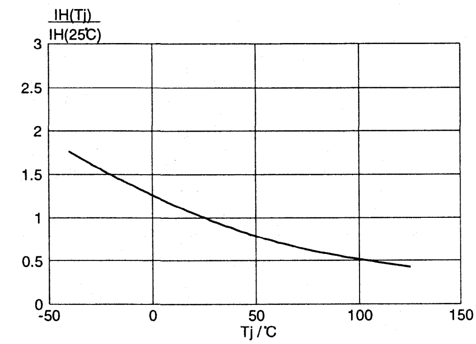


Fig.9. Normalised holding current $I_H(T_j)/\ I_H(25˚C)$, versus junction temperature T_j.

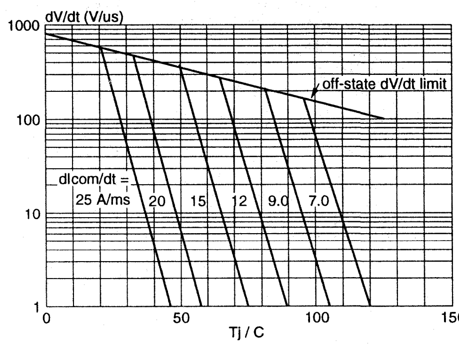


Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation dI_T/dt. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation dI_T/dt.

GENERAL DESCRIPTION

Glass passivated, sensitive gate thyristors in a plastic envelope, intended for use in general purpose switching and phase control applications.

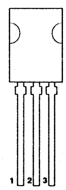
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BTA151-	**500R**	**650R**	**800R**	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages	500	650	800	V
$I_{T(AV)}$	Average on-state current	7.5	7.5	7.5	A
$I_{T(RMS)}$	RMS on-state current	12	12	12	A
I_{TSM}	Non-repetitive peak on-state current	100	100	100	A

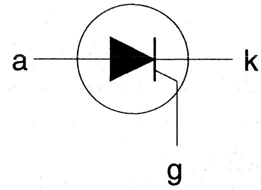
PINNING - SOT82

PIN	DESCRIPTION
1	cathode
2	anode
3	gate
tab	anode

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500R	-650R	-800R	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages		-	500[1]	650[1]	800	V
$I_{T(AV)}$	Average on-state current	half sine wave; $T_{mb} \leq 109$ ˚C	-	7.5			A
$I_{T(RMS)}$	RMS on-state current	all conduction angles	-	12			A
I_{TSM}	Non-repetitive peak on-state current	half sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$					
		t = 10 ms	-	100			A
		t = 8.3 ms	-	110			A
I^2t	I^2t for fusing	t = 10 ms	-	50			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 20$ A; $I_G = 50$ mA; $dI_G/dt = 50$ mA/µs	-	50			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
V_{RGM}	Peak reverse gate voltage		-	12			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.3	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A	-	2	4	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A	-	10	40	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	7	16	mA
V_T	On-state voltage	I_T = 23 A	-	1.4	1.75	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.6	1.5	V
		$V_D = V_{DRM(max)}$; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D, I_R	Off-state leakage current	$V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_D = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform				
		Gate open circuit	50	130	-	V/μs
		R_{GK} = 100 Ω	200	1000	-	V/μs
t_{gt}	Gate controlled turn-on time	I_{TM} = 40 A; $V_D = V_{DRM}$; I_G = 0.1 A; dI_G/dt = 5 A/μs	-	2	-	μs
t_q	Circuit commutated turn-off time	V_D = 67% $V_{DRM(max)}$; I_{TM} = 20 A; V_R = 25 V; dI_{TM}/dt = 30 A/μs; dV_D/dt = 50 V/μs; R_{GK} = 100 Ω	-	70	-	μs

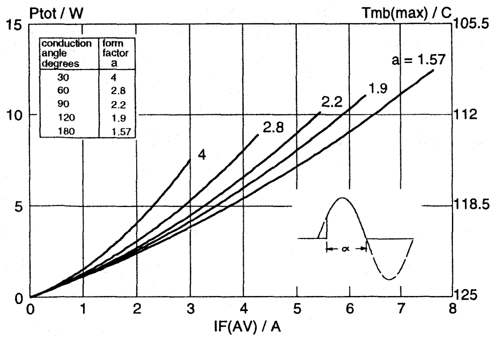


Fig.1. Maximum on-state dissipation, P_{tot}, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}/I_{T(AV)}$.

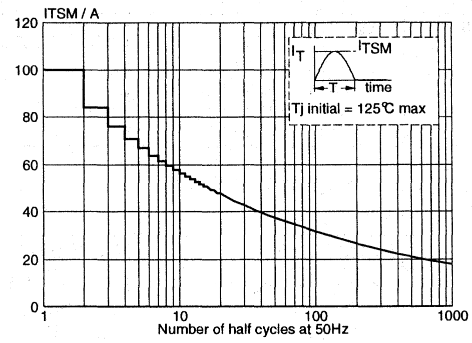


Fig.4. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

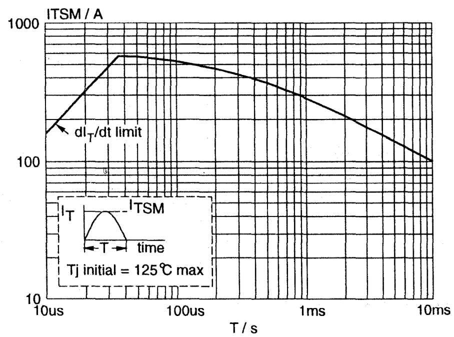


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq$ 10ms.

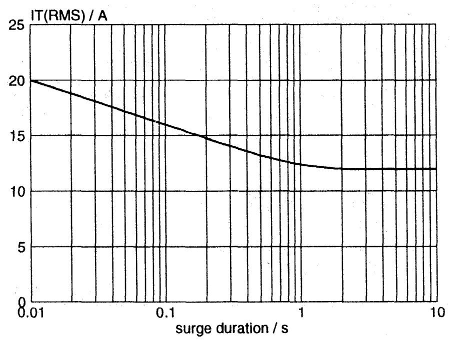


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq$ 109˚C.

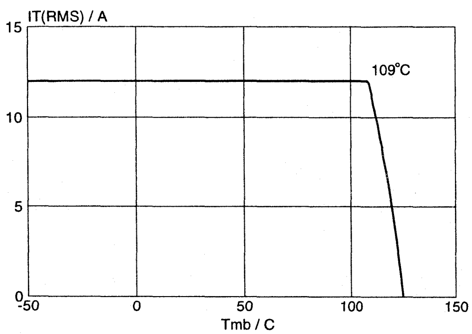


Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

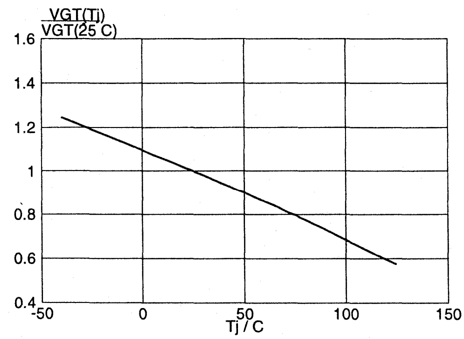


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25˚C)$, versus junction temperature T_j.

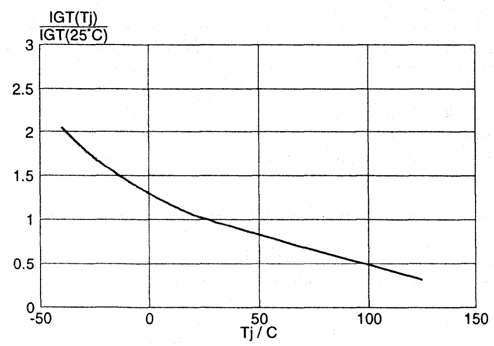


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/I_{GT}(25°C)$, versus junction temperature T_j.

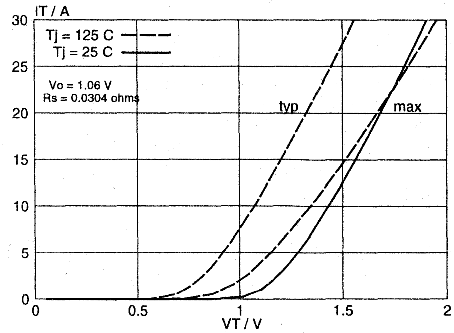


Fig.10. Typical and maximum on-state characteristic.

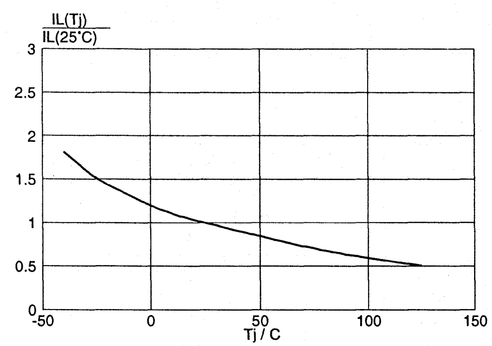


Fig.8. Normalised latching current $I_L(T_j)/I_L(25°C)$, versus junction temperature T_j.

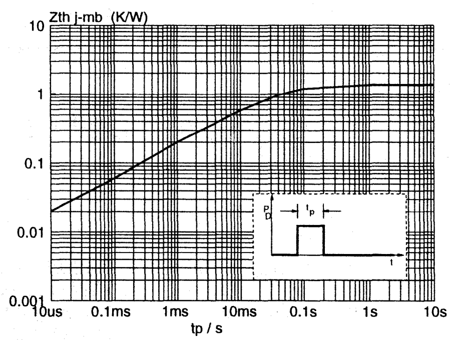


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width t_p.

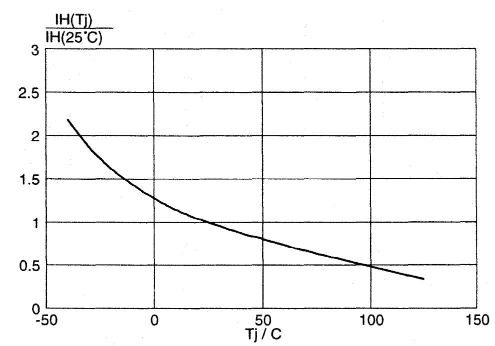


Fig.9. Normalised holding current $I_H(T_j)/I_H(25°C)$, versus junction temperature T_j.

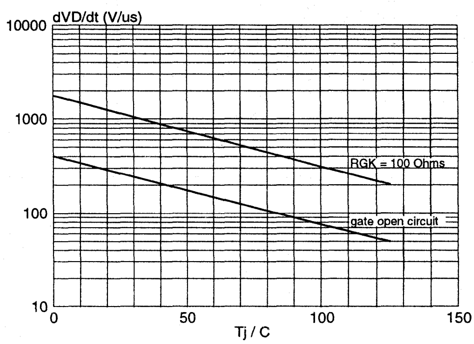


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

GENERAL DESCRIPTION

Glass passivated high commutation triacs in a plastic envelope intended for use in motor control circuits or with other highly inductive loads. These devices will commutate the full rated rms current at the maximum rated junction temperature, without the aid of a snubber.

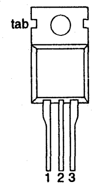
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BTA208-	600B	800B	
V_{DRM}	Repetitive peak off-state voltages	600	800	V
$I_{T(RMS)}$	RMS on-state current	8	8	A
I_{TSM}	Non-repetitive peak on-state current	55	55	A

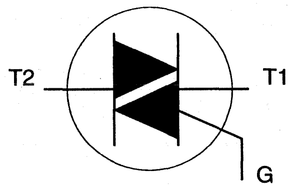
PINNING - TO220AB

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
tab	main terminal 2

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
				-600	-800	
V_{DRM}	Repetitive peak off-state voltages		-	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 102$ ˚C	-	8		A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$				
		t = 20 ms	-	55		A
		t = 16.7 ms	-	60		A
I^2t	I^2t for fusing	t = 10 ms	-	15		A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 12$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs		100		A/µs
I_{GM}	Peak gate current		-	2		A
V_{GM}	Peak gate voltage		-	5		V
P_{GM}	Peak gate power		-	5		W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5		W
T_{stg}	Storage temperature		-40	150		˚C
T_j	Operating junction temperature		-	125		˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	full cycle	-	-	2.0	K/W
		half cycle	-	-	2.4	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current[2]	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	2	18	50	mA
		T2+ G-	2	21	50	mA
		T2- G-	2	34	50	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	31	60	mA
		T2+ G-	-	34	90	mA
		T2- G-	-	30	60	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	31	60	mA
V_T	On-state voltage	I_T = 10 A	-	1.3	1.65	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	1000	4000	-	V/µs
dI_{com}/dt	Critical rate of change of commutating current	V_{DM} = 400 V; T_j = 125 ˚C; $I_{T(RMS)}$ = 8 A; without snubber; gate open circuit	-	14	-	A/ms
t_{gt}	Gate controlled turn-on time	I_{TM} = 12 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs

2 Device does not trigger in the T2-, G+ quadrant.

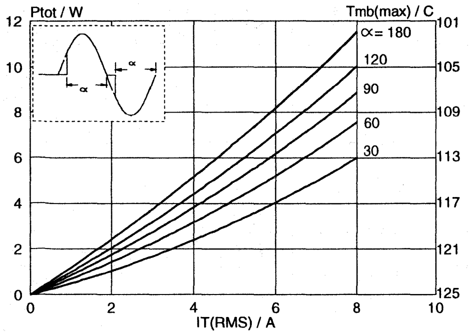


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

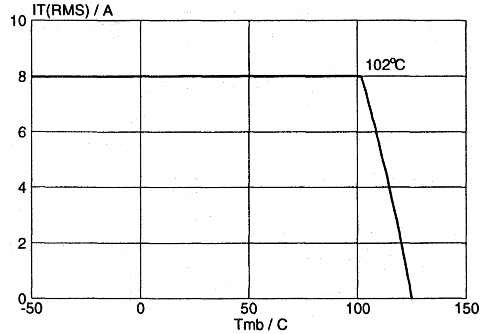


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

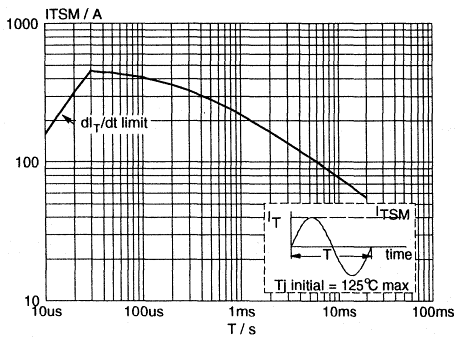


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

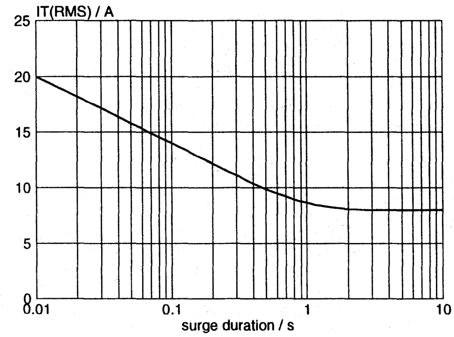


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 102^{\circ}C$.

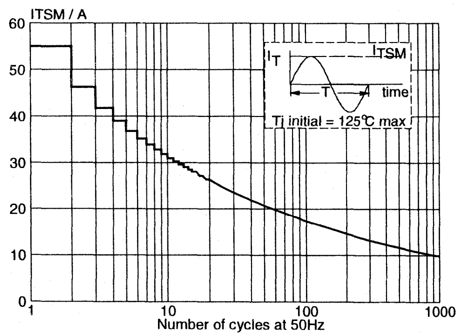


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

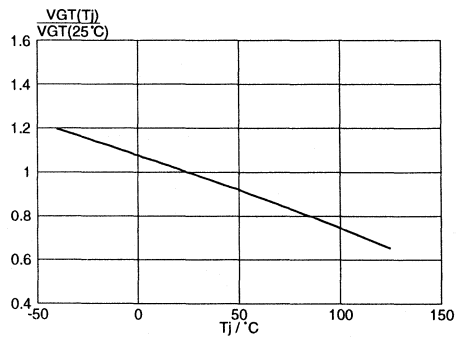


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25^{\circ}C)$, versus junction temperature T_j.

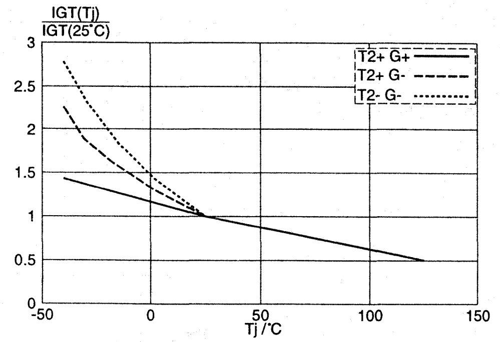


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

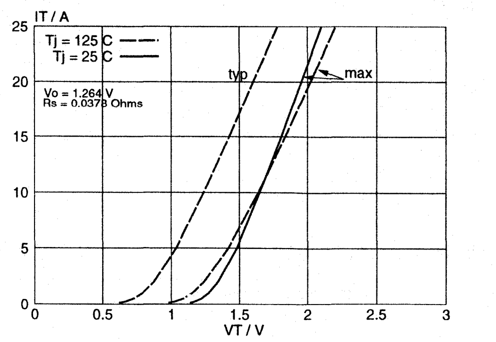


Fig.10. Typical and maximum on-state characteristic.

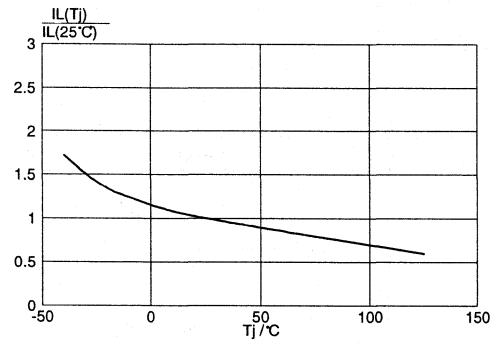


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.

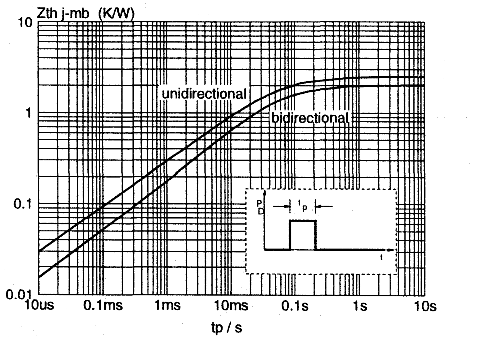


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width t_p.

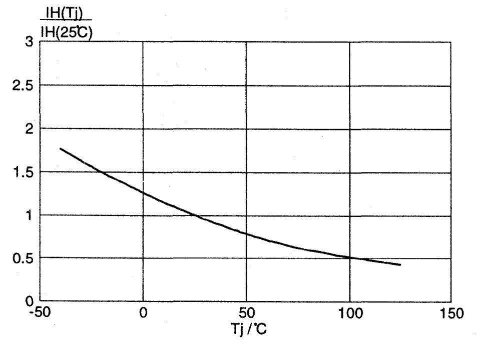


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j.

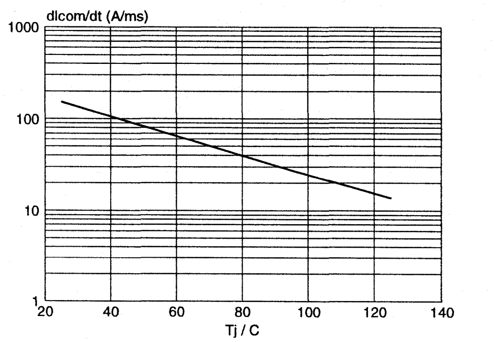


Fig.12. Typical, critical rate of change of commutating current, dI_{com}/dt versus junction temperature.

GENERAL DESCRIPTION

Glass passivated high commutation triacs in a full pack, plastic envelope intended for use in motor control circuits or with other highly inductive loads. These devices will commutate the full rated rms current at the maximum rated junction temperature, without the aid of a snubber.

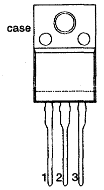
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BTA208X-	600B	800B	
V_{DRM}	Repetitive peak off-state voltages	600	800	V
$I_{T(RMS)}$	RMS on-state current	8	8	A
I_{TSM}	Non-repetitive peak on-state current	55	55	A

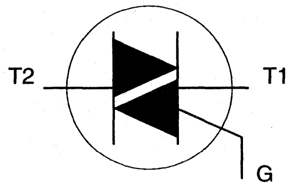
PINNING - SOT186A

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
				-600	-800	
V_{DRM}	Repetitive peak off-state voltages		-	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{hs} \leq 73$ ˚C	-	8		A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$				
		t = 20 ms	-	55		A
		t = 16.7 ms	-	60		A
I^2t	I^2t for fusing	t = 10 ms	-	15		A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 12$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs		100		A/µs
I_{GM}	Peak gate current		-	2		A
V_{GM}	Peak gate voltage		-	5		V
P_{GM}	Peak gate power		-	5		W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5		W
T_{stg}	Storage temperature		-40	150		˚C
T_j	Operating junction temperature		-	125		˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	full or half cycle with heatsink compound	-	-	4.5	K/W
		without heatsink compound	-	-	6.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current[2]	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	2	18	50	mA
		T2+ G-	2	21	50	mA
		T2- G-	2	34	50	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	31	60	mA
		T2+ G-	-	34	90	mA
		T2- G-	-	30	60	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	31	60	mA
V_T	On-state voltage	I_T = 10 A	-	1.3	1.65	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	$V_D = V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	1000	4000	-	V/µs
dI_{com}/dt	Critical rate of change of commutating current	V_{DM} = 400 V; T_j = 125 ˚C; $I_{T(RMS)}$ = 8 A; without snubber; gate open circuit	-	14	-	A/ms
t_{gt}	Gate controlled turn-on time	I_{TM} = 12 A; $V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs

2 Device does not trigger in the T2-, G+ quadrant.

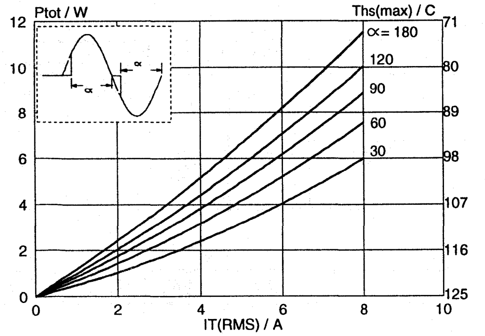


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

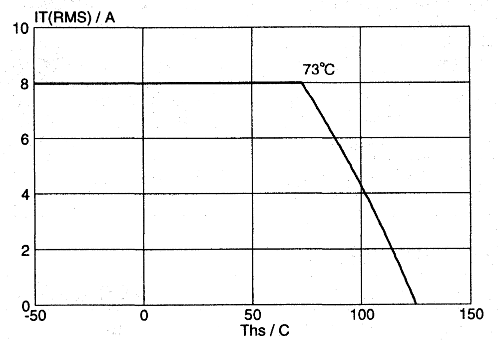


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature T_{hs}.

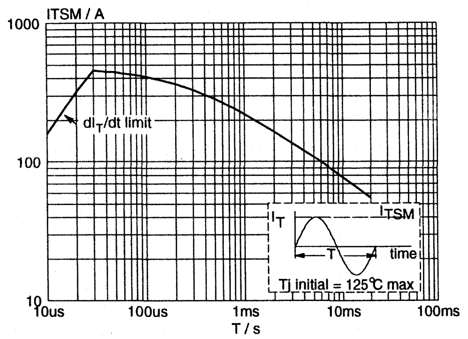


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

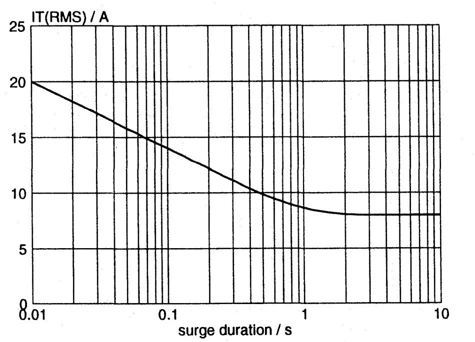


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 73^{\circ}C$.

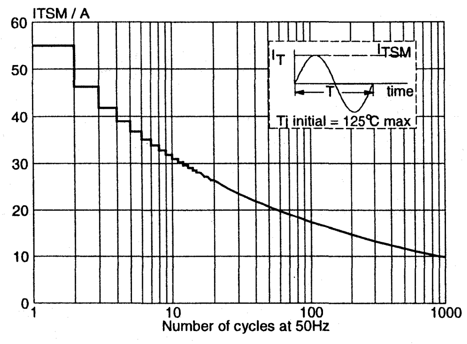


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

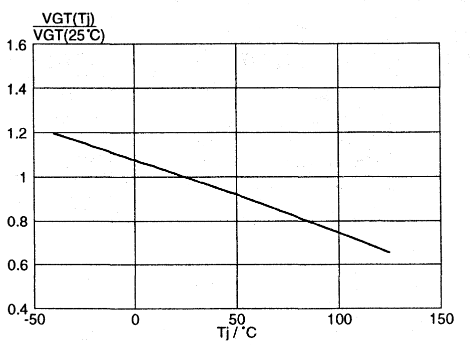


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25^{\circ}C)$, versus junction temperature T_j.

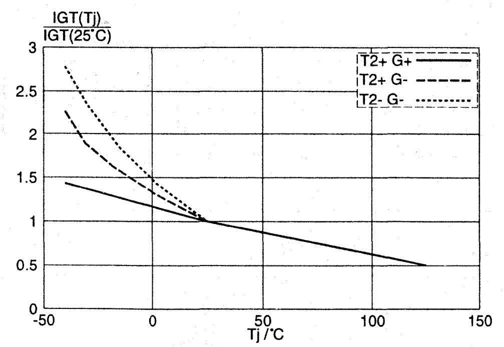


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/\ I_{GT}(25^{\circ}C)$, versus junction temperature T_j.

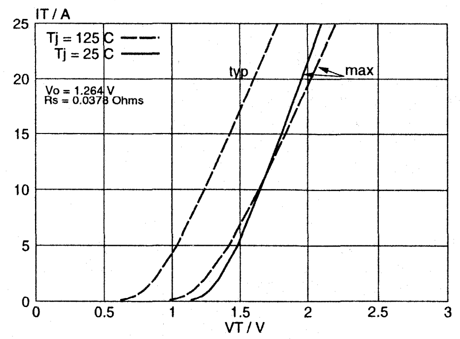


Fig.10. Typical and maximum on-state characteristic.

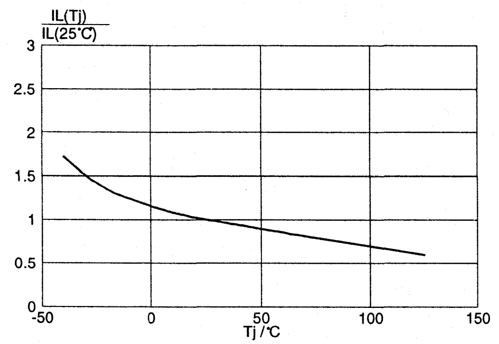


Fig.8. Normalised latching current $I_L(T_j)/\ I_L(25^{\circ}C)$, versus junction temperature T_j.

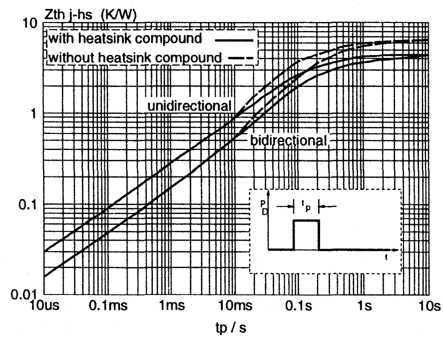


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}hs}$, versus pulse width t_p.

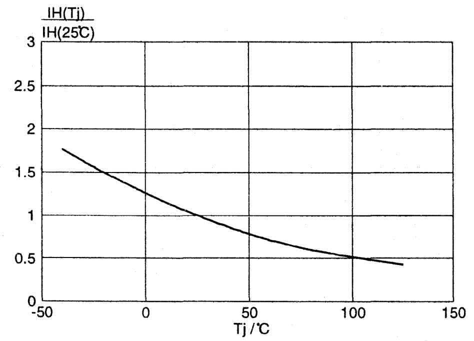


Fig.9. Normalised holding current $I_H(T_j)/\ I_H(25^{\circ}C)$, versus junction temperature T_j.

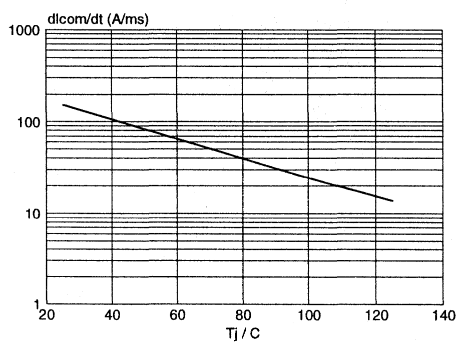


Fig.12. Typical, critical rate of change of commutating current dI_{com}/dt versus junction temperature.

Triacs high commutation | BTA212 series B

GENERAL DESCRIPTION

Glass passivated high commutation triacs in a plastic envelope intended for use in motor control circuits or with other highly inductive loads. These devices will commutate the full rated rms current at the maximum rated junction temperature, without the aid of a snubber.

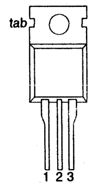
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BTA212-	**600B**	**800B**	
V_{DRM}	Repetitive peak off-state voltages	600	800	V
$I_{T(RMS)}$	RMS on-state current	12	12	A
I_{TSM}	Non-repetitive peak on-state current	90	90	A

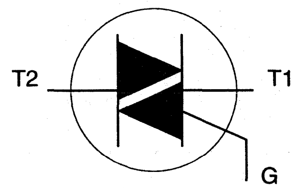
PINNING - TO220AB

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
tab	main terminal 2

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
				-600	**-800**	
V_{DRM}	Repetitive peak off-state voltages		-	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 99$ ˚C	-	12		A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$				
		t = 20 ms	-	90		A
		t = 16.7 ms	-	100		A
I^2t	I^2t for fusing	t = 10 ms	-	40		A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs		100		A/µs
I_{GM}	Peak gate current		-	2		A
V_{GM}	Peak gate voltage		-	5		V
P_{GM}	Peak gate power		-	5		W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5		W
T_{stg}	Storage temperature		-40	150		˚C
T_j	Operating junction temperature		-	125		˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	full cycle	-	-	1.5	K/W
		half cycle	-	-	2.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current[2]	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	2	18	50	mA
		T2+ G-	2	21	50	mA
		T2- G-	2	34	50	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	31	60	mA
		T2+ G-	-	34	90	mA
		T2- G-	-	30	60	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	31	60	mA
V_T	On-state voltage	I_T = 17 A	-	1.3	1.6	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	1000	4000	-	V/µs
dI_{com}/dt	Critical rate of change of commutating current	V_{DM} = 400 V; T_j = 125 ˚C; $I_{T(RMS)}$ = 12 A; without snubber; gate open circuit	-	24	-	A/ms
t_{gt}	Gate controlled turn-on time	I_{TM} = 12 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs

2 Device does not trigger in the T2-, G+ quadrant.

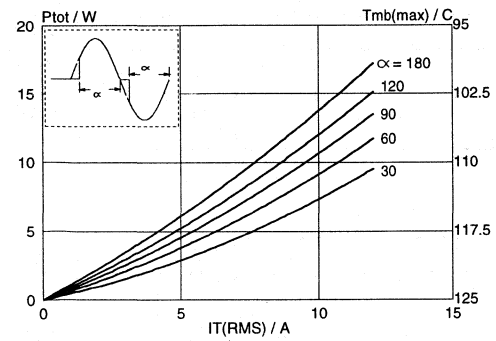


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

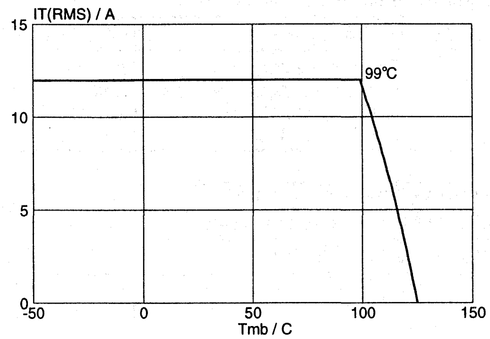


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

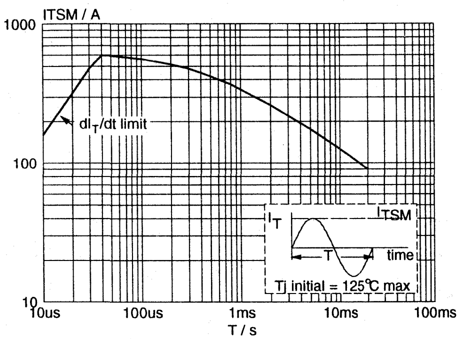


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

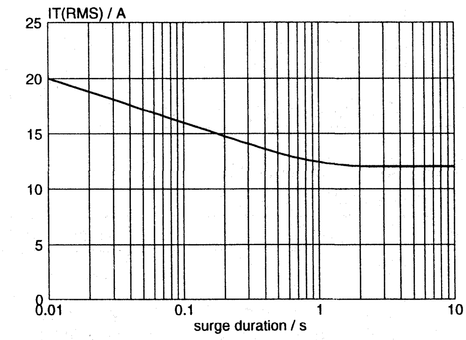


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 99$°C.

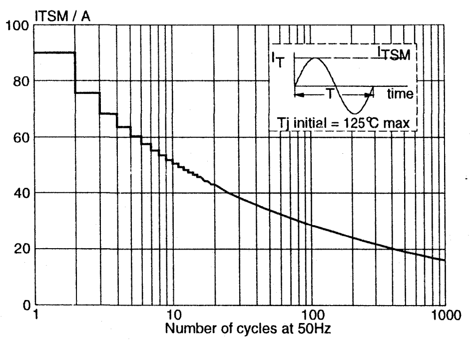


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

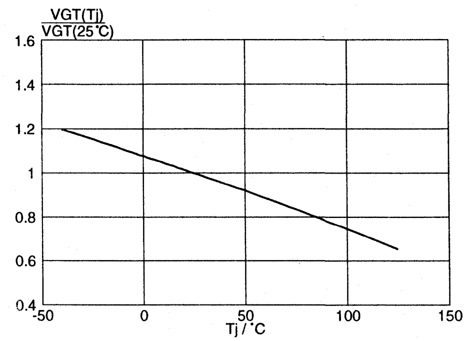


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25°C)$, versus junction temperature T_j.

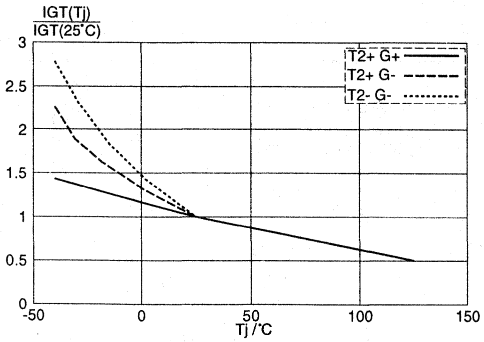


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/I_{GT}(25˚C)$, versus junction temperature T_j.

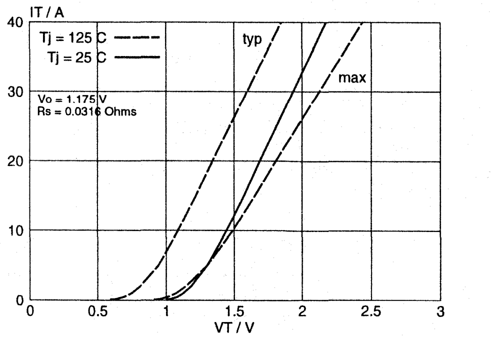


Fig.10. Typical and maximum on-state characteristic.

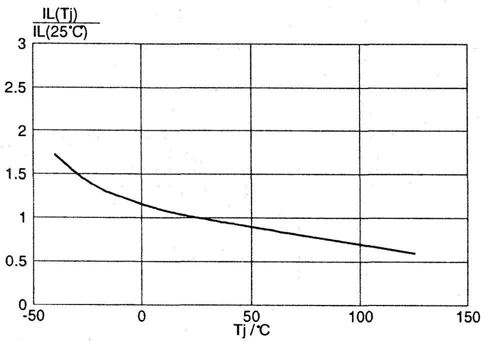


Fig.8. Normalised latching current $I_L(T_j)/I_L(25˚C)$, versus junction temperature T_j.

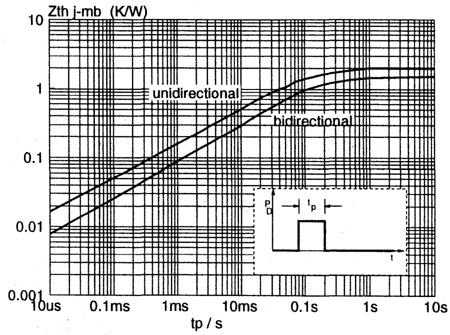


Fig.11. Transient thermal impedance $Z_{th\,j\text{-}mb}$, versus pulse width t_p.

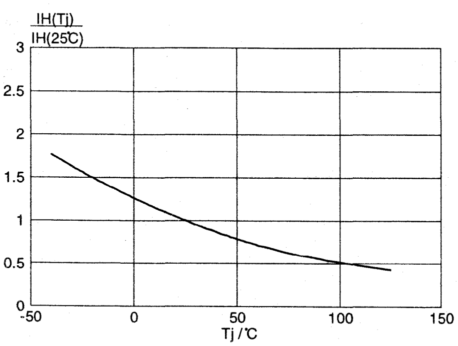


Fig.9. Normalised holding current $I_H(T_j)/I_H(25˚C)$, versus junction temperature T_j.

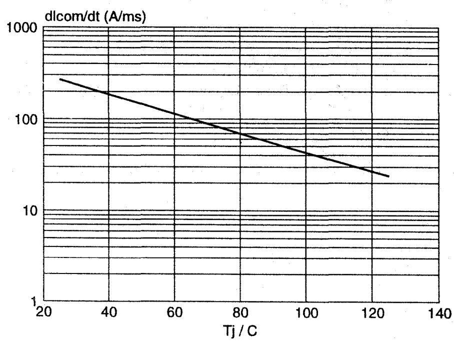


Fig.12. Typical, critical rate of change of commutating current dI_{com}/dt versus junction temperature.

GENERAL DESCRIPTION

Glass passivated high commutation triacs in a full pack, plastic envelope intended for use in motor control circuits or with other highly inductive loads. These devices will commutate the full rated rms current at the maximum rated junction temperature, without the aid of a snubber.

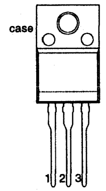
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BTA212X-	600B	800B	
V_{DRM}	Repetitive peak off-state voltages	600	800	V
$I_{T(RMS)}$	RMS on-state current	12	12	A
I_{TSM}	Non-repetitive peak on-state current	90	90	A

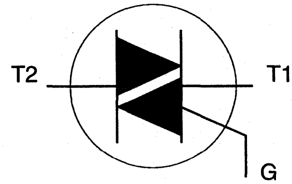
PINNING - SOT186A

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
				-600	-800	
V_{DRM}	Repetitive peak off-state voltages		-	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{hs} \leq 56$ ˚C	-	12		A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$				
		t = 20 ms	-	90		A
		t = 16.7 ms	-	100		A
I^2t	I^2t for fusing	t = 10 ms	-	40		A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs		100		A/µs
I_{GM}	Peak gate current		-	2		A
V_{GM}	Peak gate voltage		-	5		V
P_{GM}	Peak gate power		-	5		W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5		W
T_{stg}	Storage temperature		-40	150		˚C
T_j	Operating junction temperature		-	125		˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	full or half cycle				
		with heatsink compound	-	-	4.0	K/W
		without heatsink compound	-	-	5.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current[2]	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	2	18	50	mA
		T2+ G-	2	21	50	mA
		T2- G-	2	34	50	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	31	60	mA
		T2+ G-	-	34	90	mA
		T2- G-	-	30	60	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	31	60	mA
V_T	On-state voltage	I_T = 17 A	-	1.3	1.6	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	1000	4000	-	V/µs
dI_{com}/dt	Critical rate of change of commutating current	V_{DM} = 400 V; T_j = 125 ˚C; $I_{T(RMS)}$ = 12 A; without snubber; gate open circuit	-	24	-	A/ms
t_{gt}	Gate controlled turn-on time	I_{TM} = 12 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs

2 Device does not trigger in the T2-, G+ quadrant.

Triacs high commutation

BTA212X series B

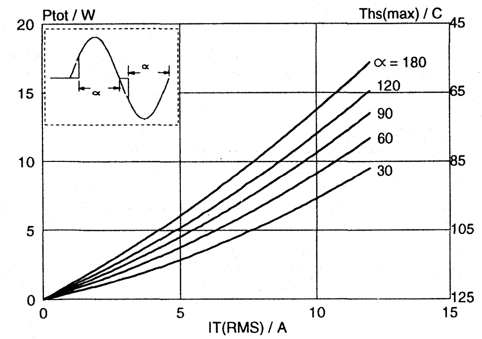


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

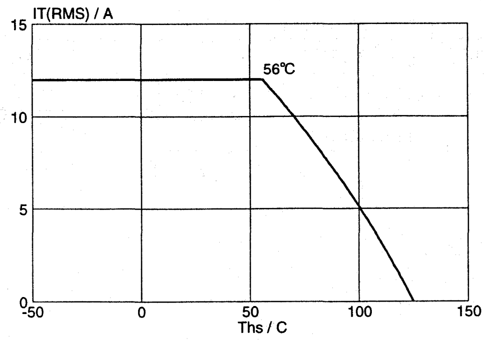


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature T_{hs}.

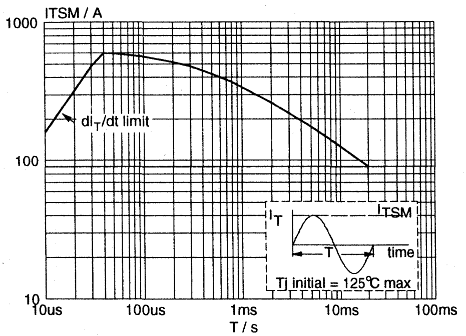


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

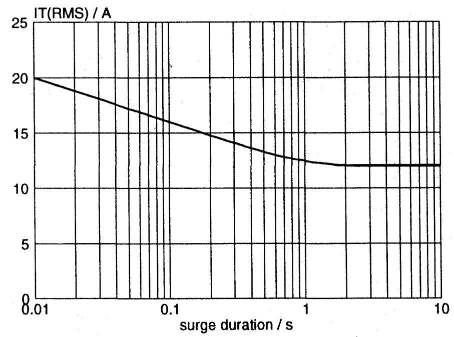


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 56^{\circ}C$.

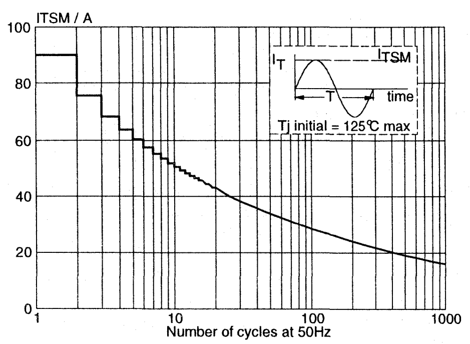


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

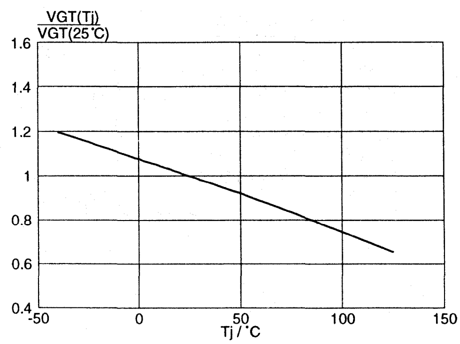


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25^{\circ}C)$, versus junction temperature T_j.

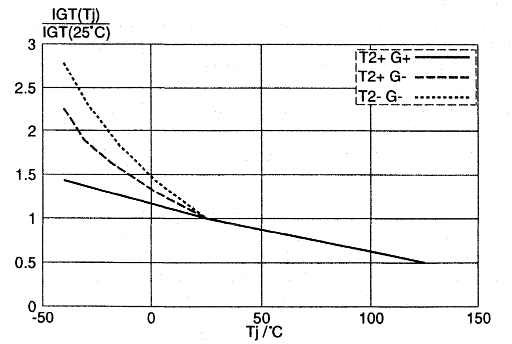


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

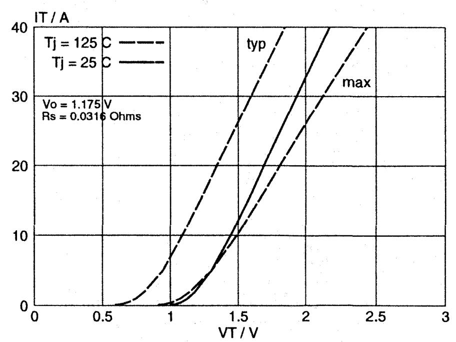


Fig.10. Typical and maximum on-state characteristic.

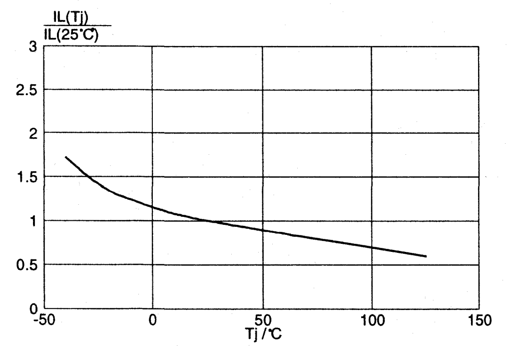


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.

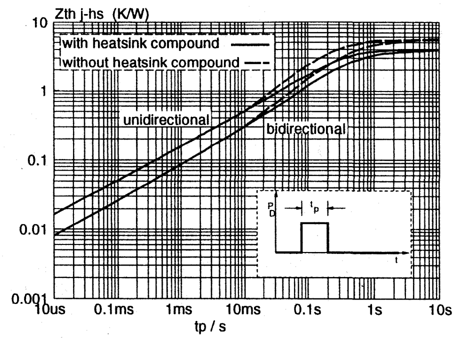


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}hs}$, versus pulse width t_p.

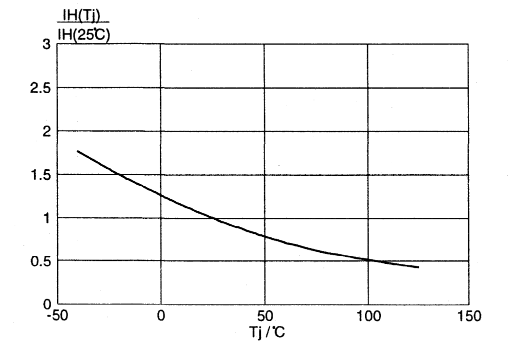


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j.

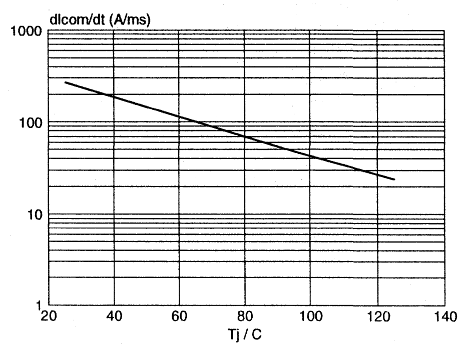


Fig.12. Typical critical rate of change of commutating current dI_{com}/dt versus junction temperature.

Triacs high commutation

GENERAL DESCRIPTION

Glass passivated high commutation triacs in a plastic envelope intended for use in motor control circuits or with other highly inductive loads. These devices will commutate the full rated rms current at the maximum rated junction temperature, without the aid of a snubber.

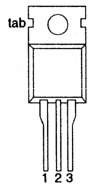
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BTA216-	**600B**	**800B**	
V_{DRM}	Repetitive peak off-state voltages	600	800	V
$I_{T(RMS)}$	RMS on-state current	16	16	A
I_{TSM}	Non-repetitive peak on-state current	140	140	A

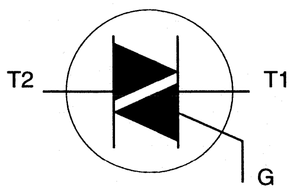
PINNING - TO220AB

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
tab	main terminal 2

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
				-600	**-800**	
V_{DRM}	Repetitive peak off-state voltages		-	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 99$ ˚C	-	16		A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$				
		t = 20 ms	-	140		A
		t = 16.7 ms	-	180		A
I^2t	I^2t for fusing	t = 10 ms	-	98		A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs		100		A/µs
I_{GM}	Peak gate current		-	2		A
V_{GM}	Peak gate voltage		-	5		V
P_{GM}	Peak gate power		-	5		W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5		W
T_{stg}	Storage temperature		-40	150		˚C
T_j	Operating junction temperature		-	125		˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	full cycle	-	-	1.2	K/W
		half cycle	-	-	1.7	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current[2]	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	2	18	50	mA
		T2+ G-	2	21	50	mA
		T2- G-	2	34	50	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	31	60	mA
		T2+ G-	-	34	90	mA
		T2- G-	-	30	60	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	31	60	mA
V_T	On-state voltage	I_T = 20 A	-	1.2	1.5	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	$V_D = V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	1000	4000	-	V/μs
dI_{com}/dt	Critical rate of change of commutating current	V_{DM} = 400 V; T_j = 125 ˚C; $I_{T(RMS)}$ = 16 A; without snubber; gate open circuit	-	28	-	A/ms
t_{gt}	Gate controlled turn-on time	I_{TM} = 20 A; $V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/μs	-	2	-	μs

2 Device does not trigger in the T2-, G+ quadrant.

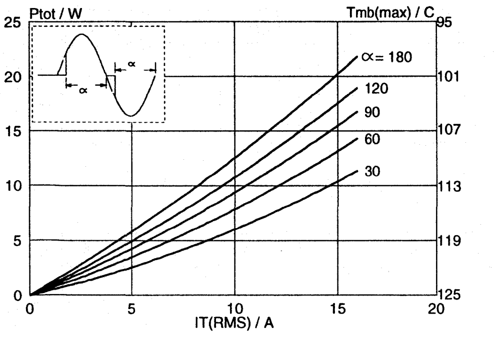


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

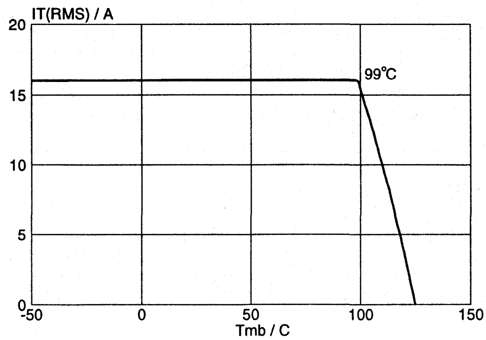


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

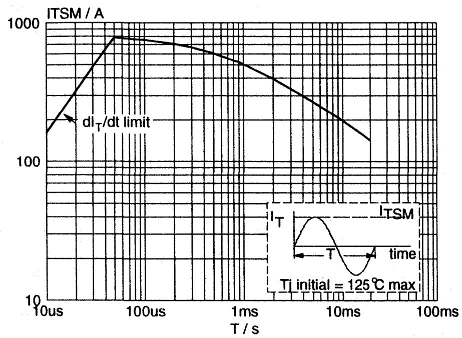


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

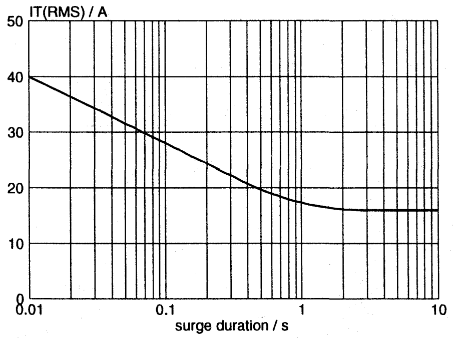


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 99°C$.

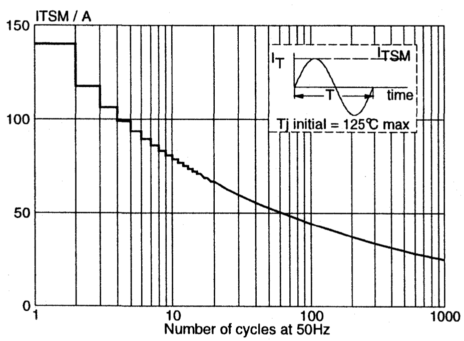


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

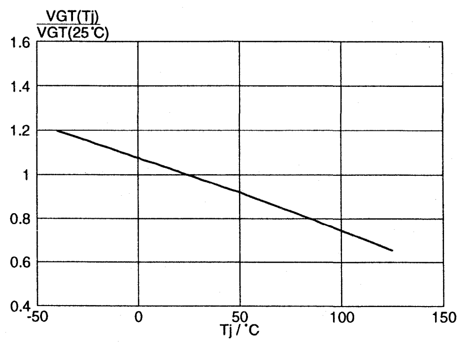


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature T_j.

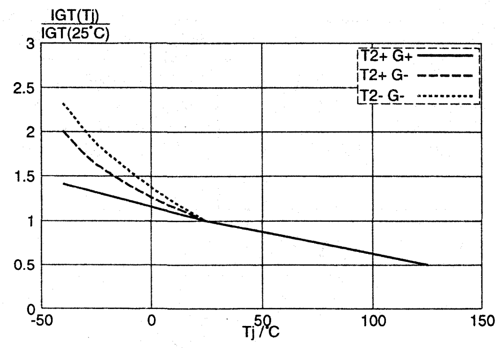


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25^{\circ}C)$, versus junction temperature T_j.

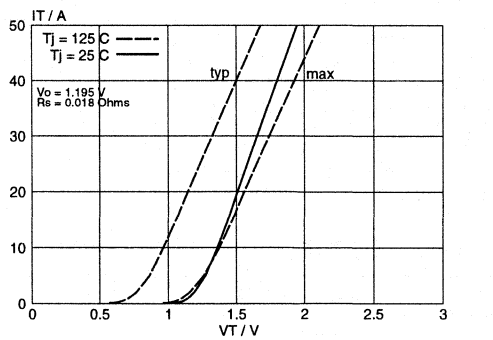


Fig.10. Typical and maximum on-state characteristic.

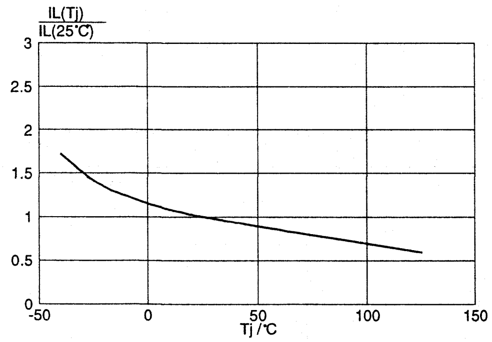


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25^{\circ}C)$, versus junction temperature T_j.

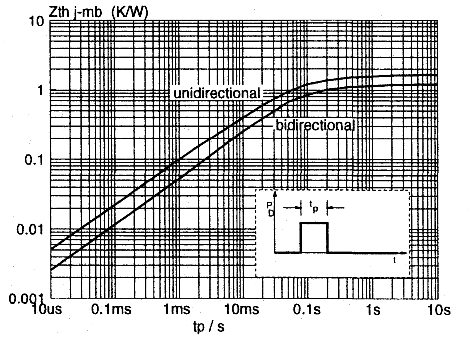


Fig.11. Transient thermal impedance $Z_{th\,j\text{-}mb}$, versus pulse width t_p.

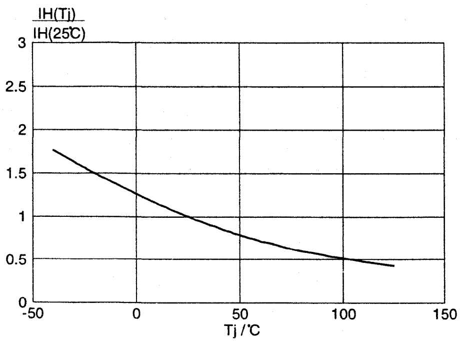


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25^{\circ}C)$, versus junction temperature T_j.

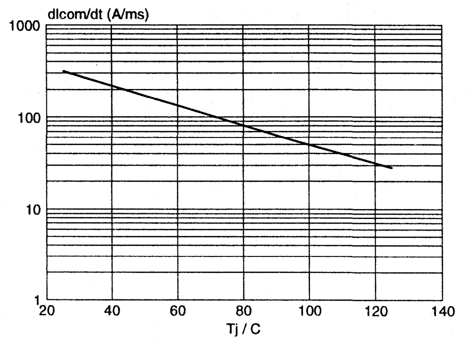


Fig.12. Typical, critical rate of change of commutating current dI_{com}/dt versus junction temperature.

Triacs high commutation

BTA216X series B

GENERAL DESCRIPTION

Glass passivated high commutation triacs in a full pack, plastic envelope intended for use in motor control circuits or with other highly inductive loads. These devices will commutate the full rated rms current at the maximum rated junction temperature, without the aid of a snubber.

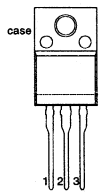
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BTA216X-	**600B**	**800B**	
V_{DRM}	Repetitive peak off-state voltages	600	800	V
$I_{T(RMS)}$	RMS on-state current	16	16	A
I_{TSM}	Non-repetitive peak on-state current	140	140	A

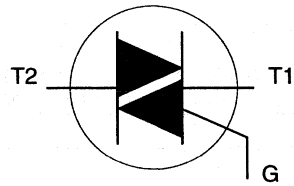
PINNING - SOT186A

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
				-600	**-800**	
V_{DRM}	Repetitive peak off-state voltages		-	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{hs} \leq 38$ ˚C	-	16		A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$				
		t = 20 ms	-	140		A
		t = 16.7 ms	-	180		A
I^2t	I^2t for fusing	t = 10 ms	-	98		A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/μs		100		A/μs
I_{GM}	Peak gate current		-	2		A
V_{GM}	Peak gate voltage		-	5		V
P_{GM}	Peak gate power		-	5		W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5		W
T_{stg}	Storage temperature		-40	150		˚C
T_j	Operating junction temperature		-	125		˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/μs.

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	full or half cycle				
		with heatsink compound	-	-	4.0	K/W
		without heatsink compound	-	-	5.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current[2]	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	2	18	50	mA
		T2+ G-	2	21	50	mA
		T2- G-	2	34	50	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	31	60	mA
		T2+ G-	-	34	90	mA
		T2- G-	-	30	60	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	31	60	mA
V_T	On-state voltage	I_T = 20 A	-	1.2	1.5	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	$V_D = V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	1000	4000	-	V/µs
dI_{com}/dt	Critical rate of change of commutating current	V_{DM} = 400 V; T_j = 125 ˚C; $I_{T(RMS)}$ = 16 A; without snubber; gate open circuit	-	28	-	A/ms
t_{gt}	Gate controlled turn-on time	I_{TM} = 20 A; $V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs

2 Device does not trigger in the T2-, G+ quadrant.

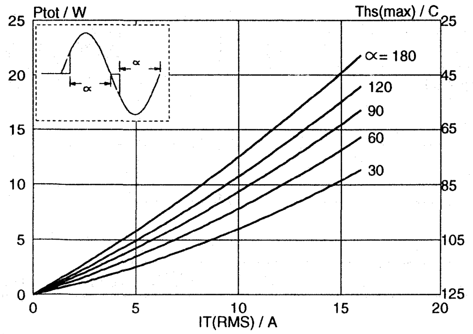


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

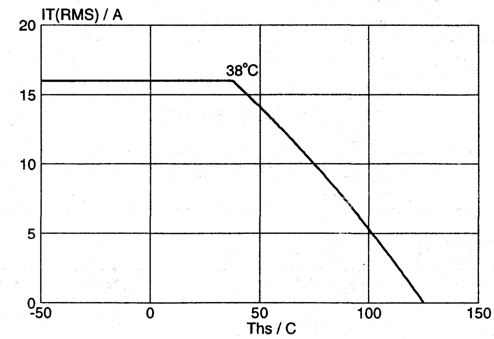


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature T_{hs}.

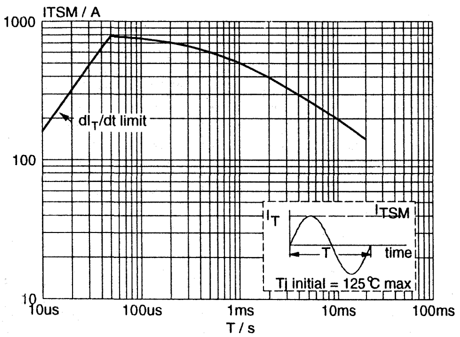


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq$ 20ms.

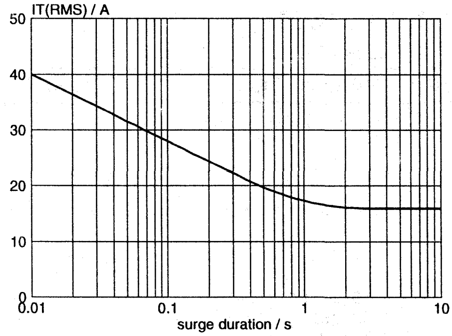


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq$ 38˚C.

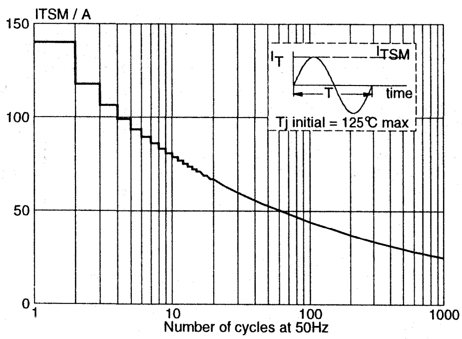


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

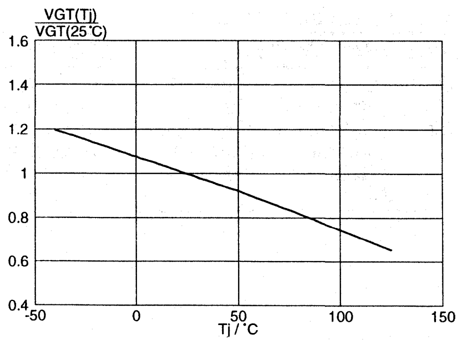


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)$/ V_{GT}(25˚C), versus junction temperature T_j.

Triacs high commutation

BTA216X series B

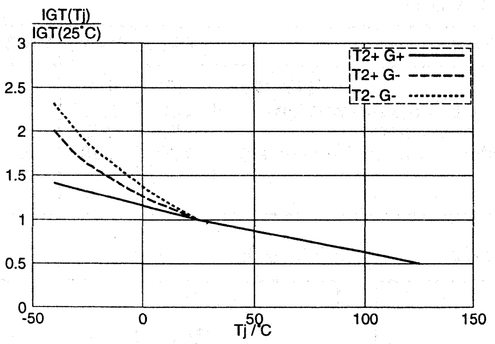


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/\ I_{GT}(25˚C)$, versus junction temperature T_j.

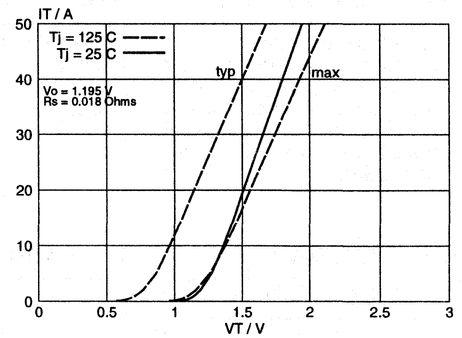


Fig.10. Typical and maximum on-state characteristic.

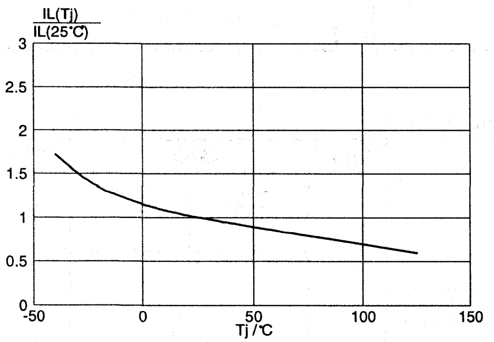


Fig.8. Normalised latching current $I_L(T_j)/\ I_L(25˚C)$, versus junction temperature T_j.

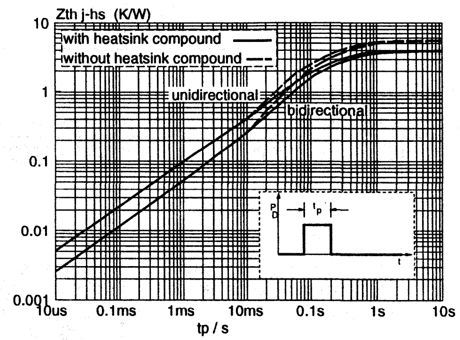


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width t_p.

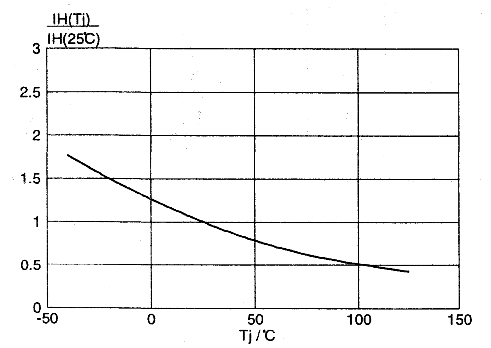


Fig.9. Normalised holding current $I_H(T_j)/\ I_H(25˚C)$, versus junction temperature T_j.

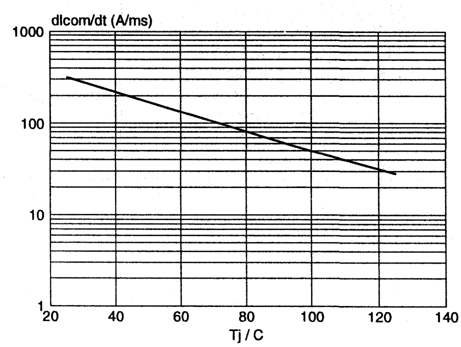


Fig.12. Typical, critical rate of change of commutating current dI_{com}/dt versus junction temperature.

GENERAL DESCRIPTION

Glass passivated high commutation triacs in a plastic envelope intended for use in motor control circuits or with other highly inductive loads. These devices will commutate the full rated rms current at the maximum rated junction temperature, without the aid of a snubber.

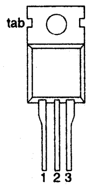
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BTA225-	600B	800B	
V_{DRM}	Repetitive peak off-state voltages	600	800	V
$I_{T(RMS)}$	RMS on-state current	25	25	A
I_{TSM}	Non-repetitive peak on-state current	180	180	A

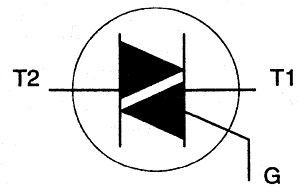
PINNING - TO220AB

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
tab	main terminal 2

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
				-600	-800	
V_{DRM}	Repetitive peak off-state voltages		-	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 91$ ˚C	-	25		A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 125$ ˚C prior to surge; with reapplied $V_{DRM(max)}$				
		t = 20 ms	-	180		A
		t = 16.7 ms	-	200		A
I^2t	I^2t for fusing	t = 10 ms	-	160		A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 30$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs		100		A/µs
I_{GM}	Peak gate current		-	2		A
V_{GM}	Peak gate voltage		-	5		V
P_{GM}	Peak gate power		-	5		W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5		W
T_{stg}	Storage temperature		-40	150		˚C
T_j	Operating junction temperature		-	125		˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	full cycle	-	-	1.0	K/W
		half cycle	-	-	1.4	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current[2]	V_D = 12 V; I_T = 0.1 A				
		T2+ G+	2	18	50	mA
		T2+ G-	2	21	50	mA
		T2- G-	2	34	50	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A				
		T2+ G+	-	31	60	mA
		T2+ G-	-	34	90	mA
		T2- G-	-	30	60	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	31	60	mA
V_T	On-state voltage	I_T = 30 A	-	1.2	1.55	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-	V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	1000	4000	-	V/µs
dI_{com}/dt	Critical rate of change of commutating current	V_{DM} = 400 V; T_j = 125 ˚C; $I_{T(RMS)}$ = 25 A; without snubber; gate open circuit	-	44	-	A/ms
t_{gt}	Gate controlled turn-on time	I_{TM} = 30 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs

2 Device does not trigger in the T2-, G+ quadrant.

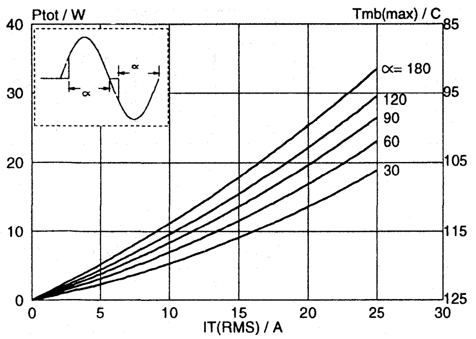


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

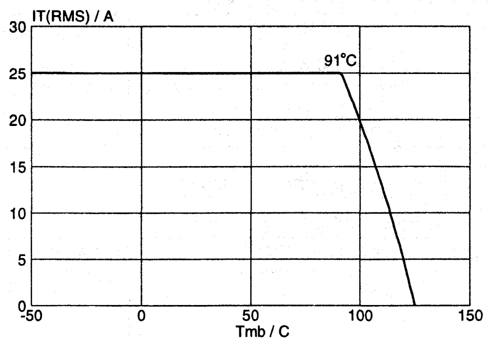


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

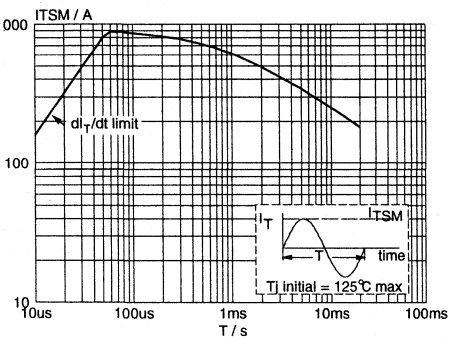


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq$ 20ms.

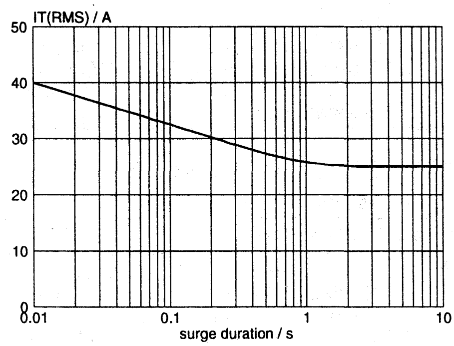


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq$ 91˚C.

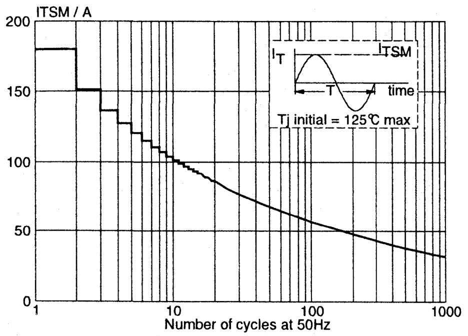


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

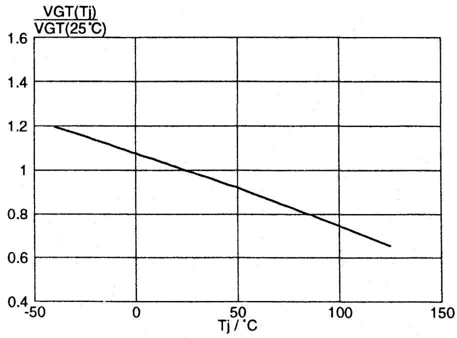


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)$/ V_{GT}(25˚C), versus junction temperature T_j.

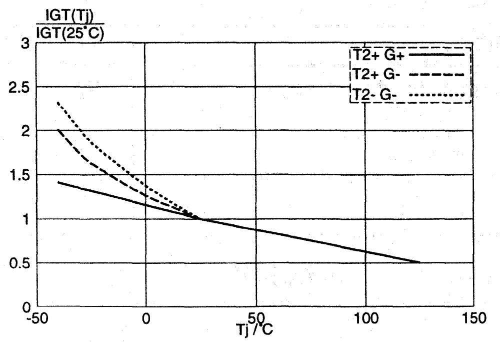


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/\ I_{GT}(25˚C)$, versus junction temperature T_j.

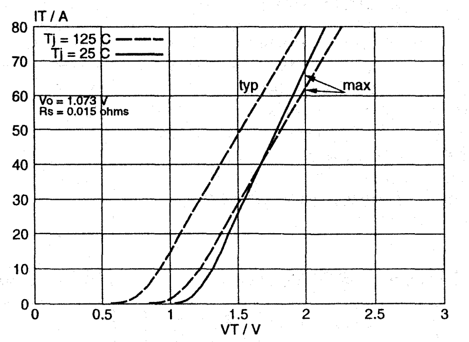


Fig.10. Typical and maximum on-state characteristic.

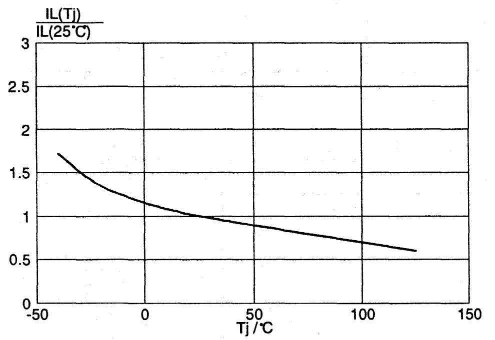


Fig.8. Normalised latching current $I_L(T_j)/\ I_L(25˚C)$, versus junction temperature T_j.

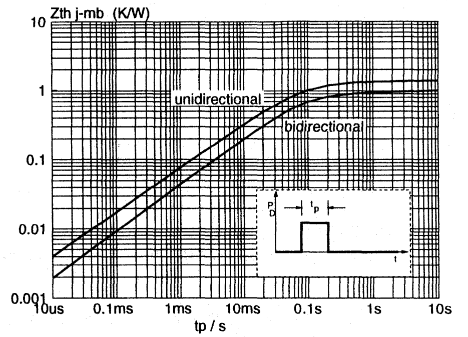


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width t_p.

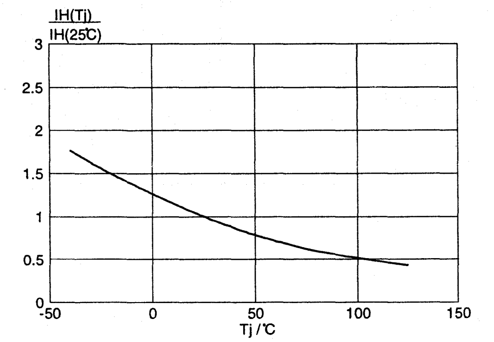


Fig.9. Normalised holding current $I_H(T_j)/\ I_H(25˚C)$, versus junction temperature T_j.

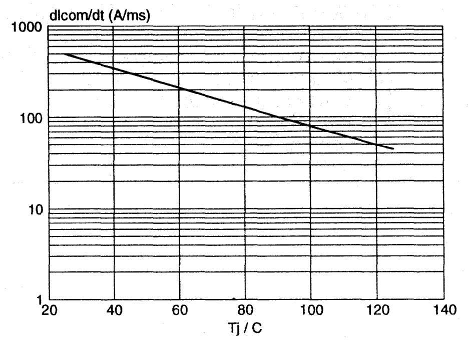


Fig.12. Typical, critical rate of change of commutating current dI_{com}/dt versus junction temperature.

Thyristor sensitive gate | 2N5064

GENERAL DESCRIPTION

Glass passivated sensitive gate thyristor in a plastic envelope, intended for use in general purpose switching and phase control applications. This device is intended to be interfaced directly to microcontrollers, logic integreated circuits and other low power gate trigger circuits.

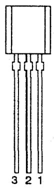
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages	200	V
$I_{T(AV)}$	Average on-state current	0.5	A
$I_{T(RMS)}$	RMS on-state current	0.8	A
I_{TSM}	Non-repetitive peak on-state current	10	A

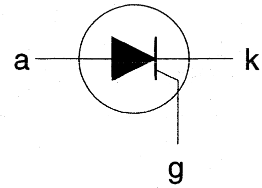
PINNING - TO92 variant

PIN	DESCRIPTION
1	anode
2	gate
3	cathode

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages		-	200	V
$I_{T(AV)}$	Average on-state current	half sine wave			
		$T_c \leq 67$ ˚C	-	0.51	A
		$T_c \leq 102$ ˚C	-	0.255	A
$I_{T(RMS)}$	RMS on-state current	all conduction angles	-	0.8	A
I_{TRM}	Repetitive peak on-state current		-	8	A
I_{TSM}	Non-repetitive peak on-state current	half sine wave; $T_a = 25$ ˚C prior to surge; with reapplied $V_{DRM(max)}$; t = 8.3 ms	-	10	A
I^2t	I^2t for fusing	t = 8.3 ms	-	0.4	A^2s
I_{GM}	Peak gate current	$T_a = 25$˚C, $t_p = 300$µs; f = 120 Hz	-	1	A
V_{GM}	Peak gate voltage		-	5	V
V_{RGM}	Peak reverse gate voltage		-	5	V
P_{GM}	Peak gate power	$T_a = 25$˚C	-	0.1	W
$P_{G(AV)}$	Average gate power	$T_a = 25$˚C, over any 16 ms period	-	0.01	W
T_{stg}	Storage temperature		-65	150	˚C
T_j	Operating junction temperature		-65	125	˚C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}c}$	Thermal resistance junction to case	see note:[1]	-	-	75	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	200	-	K/W

STATIC CHARACTERISTICS

T_c = 25 ˚C, R_{GK} = 1 kΩ unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	T_c = 25 ˚C	-	-	200	µA
		T_c = -65 ˚C	-	-	350	µA
		$V_D = V_{DRM(max)}$; R_L = 100 Ω; gate open circuit				
I_L	Latching current	V_D = 12 V; R_{GK} = 1 kΩ	-	-	6	mA
I_H	Holding current	V_D = 12 V; R_{GK} = 1 kΩ	-	-	5	mA
V_T	On-state voltage	I_T = 1.2 A peak; t_p = 300 µs; $\delta \leq 0.01$	-	-	1.7	V
V_{GT}	Gate trigger voltage	T_j = 25 ˚C	-	-	0.8	V
		T_j = -65 ˚C	-	-	1.2	V
		T_j = 125 ˚C	0.1	-	-	V
		$V_D = V_{DRM(max)}$; R_L = 100 Ω; gate open circuit				
I_D, I_R	Off-state leakage current	$V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$				
		T_j = 25 ˚C	-	-	10	µA
		T_j = 125 ˚C	-	-	50	µA

DYNAMIC CHARACTERISTICS

T_c = 25 ˚C, R_{GK} = 1 kΩ unless otherwise stated

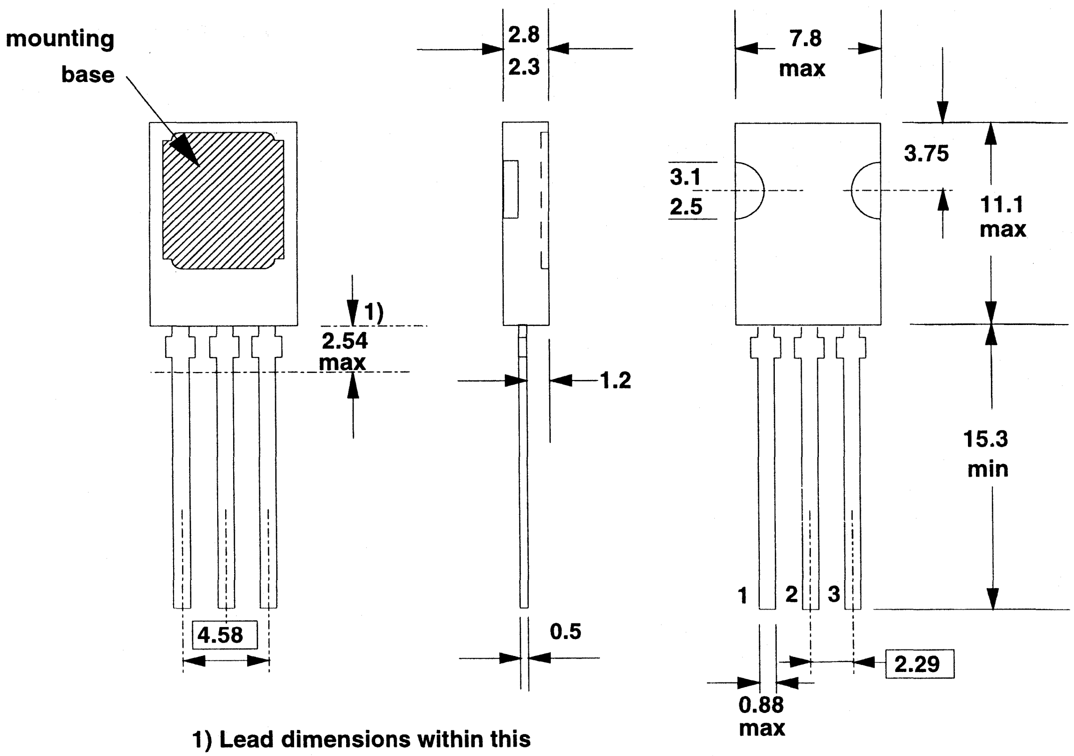
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; R_{GK} = 1 kΩ	-	25	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 2 A; $V_D = V_{DRM(max)}$; I_G = 10 mA; dI_G/dt = 0.1 A/µs	-	2	-	µs
t_q	Circuit commutated turn-off time	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; I_{TM} = 1.6 A; V_R = 35 V; dI_{TM}/dt = 30 A/µs; dV_D/dt = 2 V/µs; R_{GK} = 1 kΩ	-	100	-	µs

1 This measurement is made with the case mounted "flat side down" on a heatsink and held in position by means of a metal clamp over the curved surface.

MECHANICAL DATA

Dimensions in mm

Net Mass: 0.8 g



1) Lead dimensions within this zone uncontrolled.

Fig.13. SOT82; pin 2 connected to mounting base.

Notes

1. Refer to mounting instructions for SOT82 envelopes.
2. Epoxy meets UL94 V0 at 1/8".

Dimensions in mm

Net Mass: 2 g

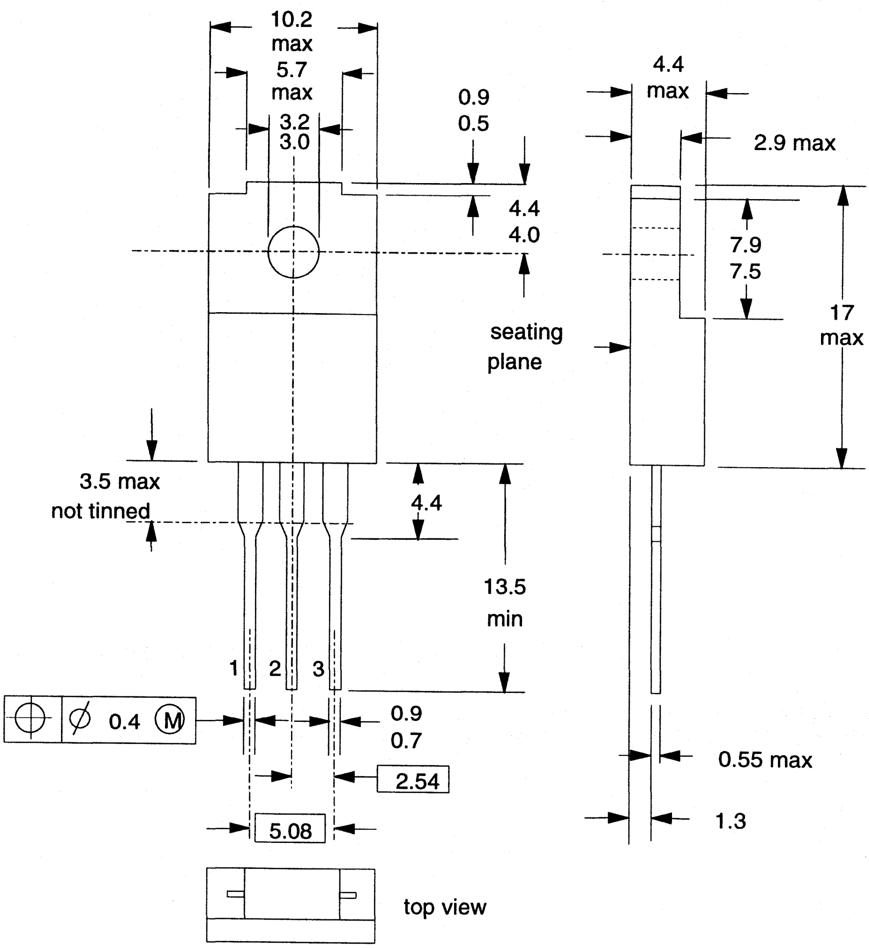


Fig. 13. SOT186; The seating plane is electrically isolated from all terminals.

Notes
1. Accessories supplied on request: refer to mounting instructions for F-pack envelopes.
2. Epoxy meets UL94 V0 at 1/8".

Dimensions in mm

Net Mass: 2 g

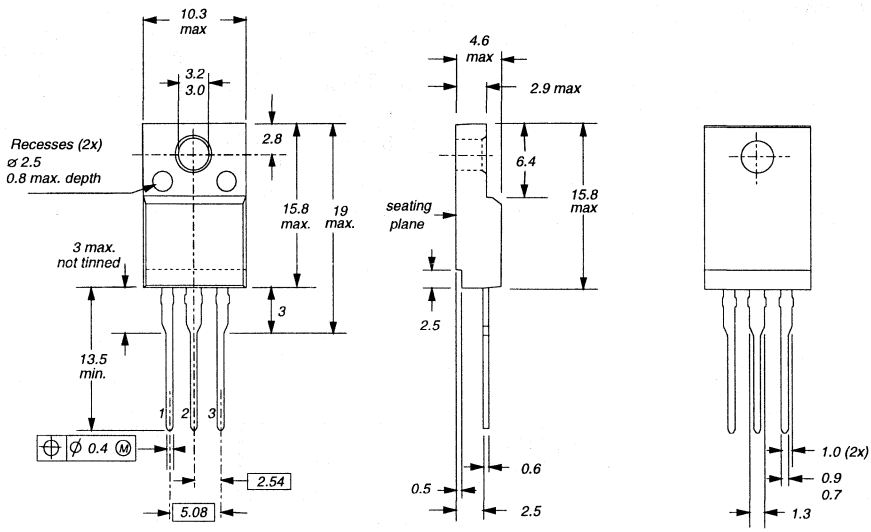


Fig. 13. SOT186A; The seating plane is electrically isolated from all terminals.

Notes
1. Accessories supplied on request: refer to mounting instructions for F-pack envelopes.
2. The improved isolation rating applies only to the SOT186 version A envelope.

Dimensions in mm

Net Mass: 0.11 g

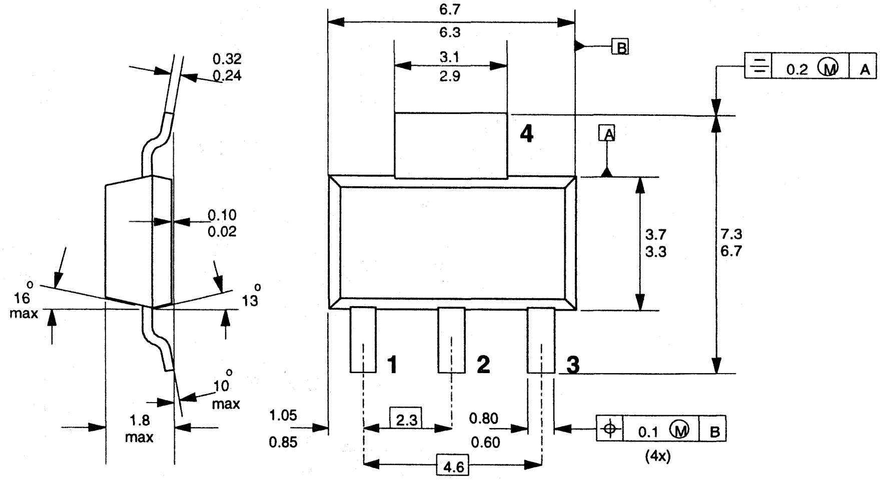


Fig.15. SOT223 surface mounting package.

Notes

1. For further information, refer to surface mounting instructions for SOT223 envelope.
2. Epoxy meets UL94 V0 at 1/8".

Dimensions in mm

Net Mass: 0.2 g

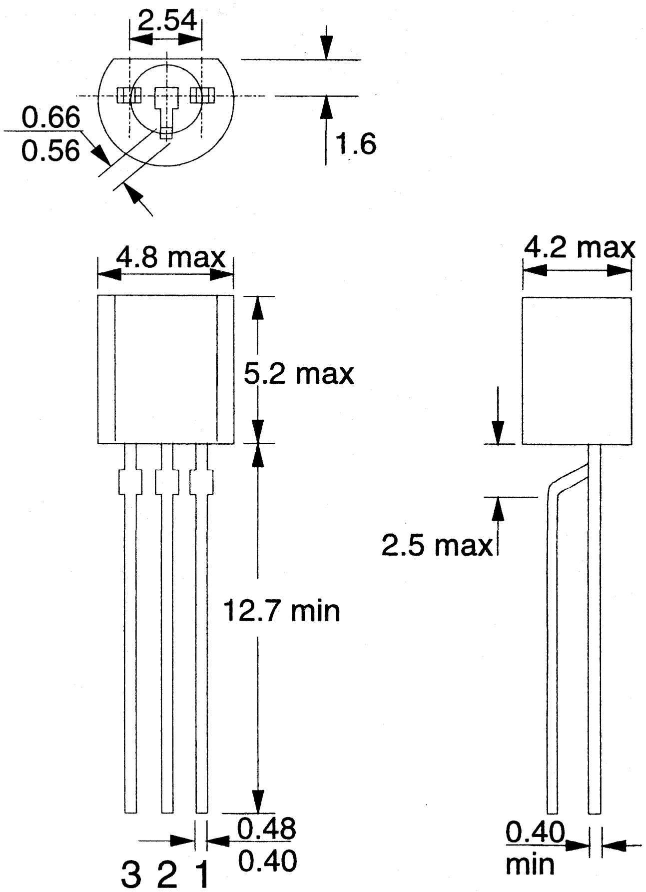


Fig.1. TO92; plastic envelope.

Notes

1. Epoxy meets UL94 V0 at 1/8".

Dimensions in mm

Net Mass: 2 g

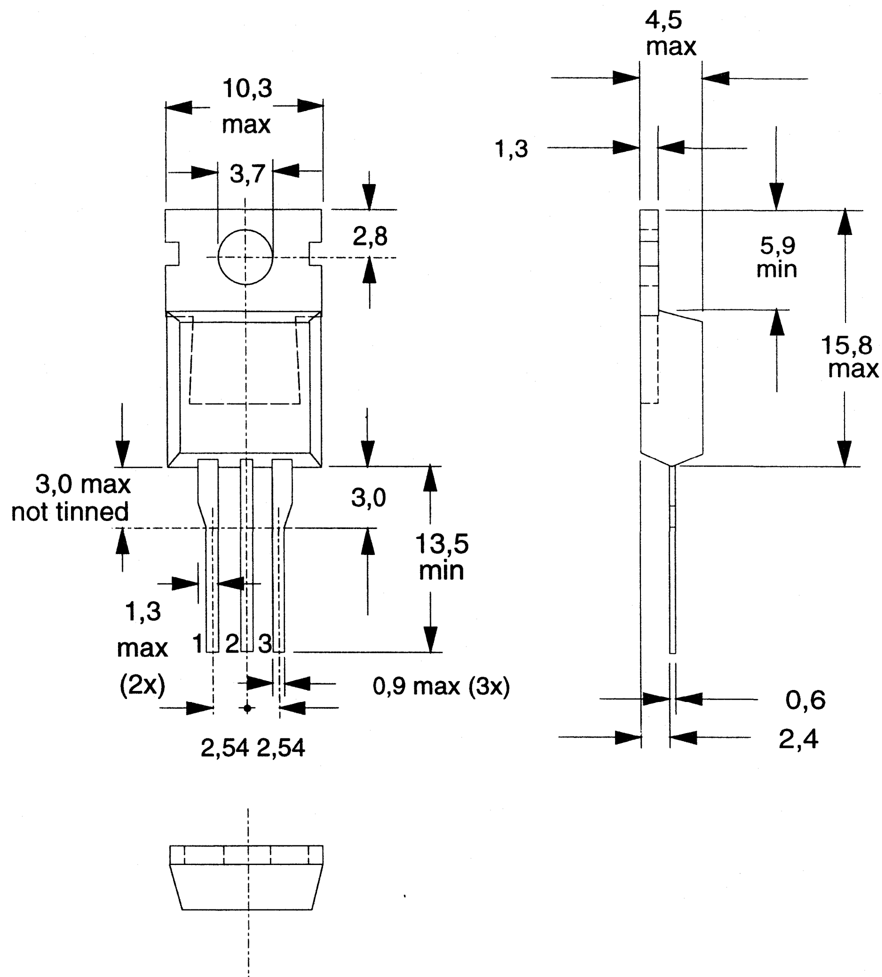


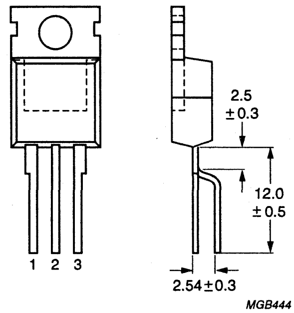
Fig.13. TO220AB; pin 2 connected to mounting base.

Notes
1. Accessories supplied on request: refer to mounting instructions for TO220 envelopes.
2. Epoxy meets UL94 V0 at 1/8".

LEADFORM OPTIONS

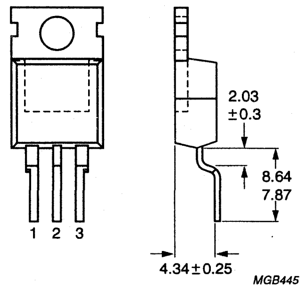
LEADFORM OPTIONS

- These options require a special part number before ordering.
- Contact your local Philips Semiconductors representative for pricing, minimum order quantities and part number.



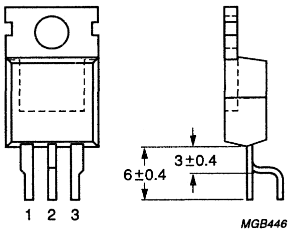
SOT78 (TO-220)

Fig.1 Leadform 78-02.



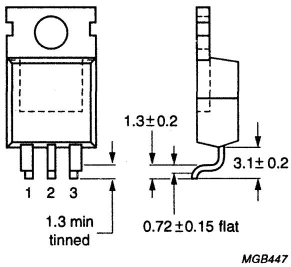
SOT78 (TO-220)

Fig.2 Leadform 78-05W.



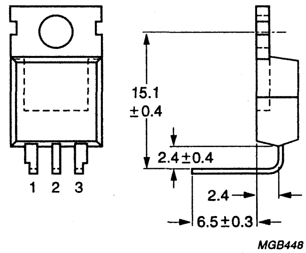
SOT78 (TO-220)

Fig.3 Leadform 78-13.



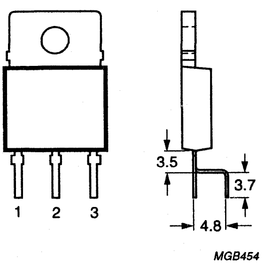
SOT78 (TO-220)

Fig.4 Leadform 78-14.



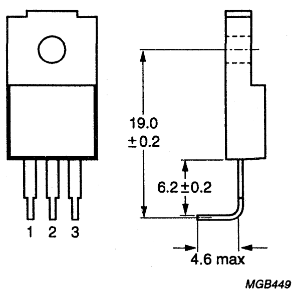
SOT78 (TO-220)

Fig.5 Leadform 78-15.



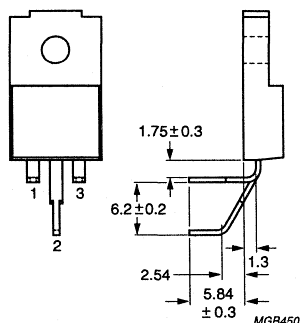
SOT93

Fig.6 Leadform 93-01.



SOT186

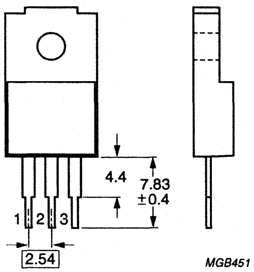
Fig.7 Leadform 186-01A.



SOT186

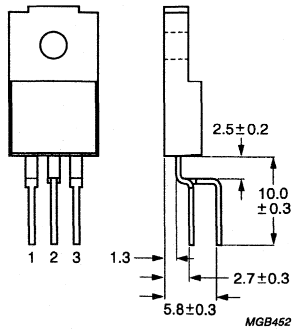
Fig.8 Leadform 186-01B.

Leadform options



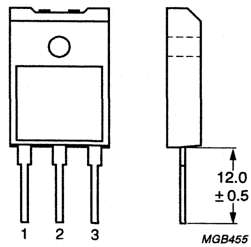
SOT186

Fig.9 Leadform 186-02.



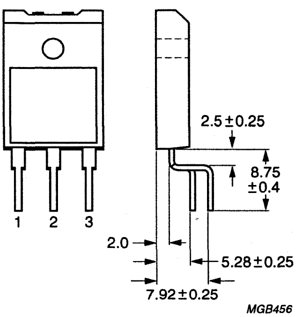
SOT186

Fig.10 Leadform 186A-02.



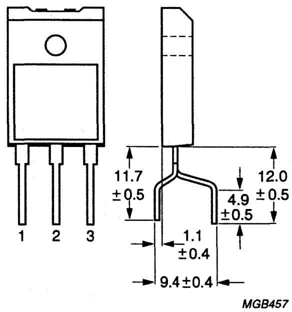
SOT199

Fig.11 Leadform 199-01.



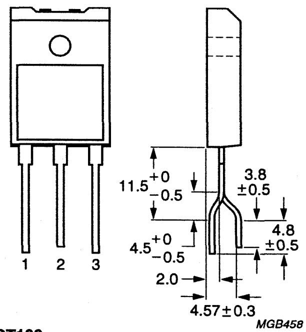
SOT199

Fig.12 Leadform 199-02.



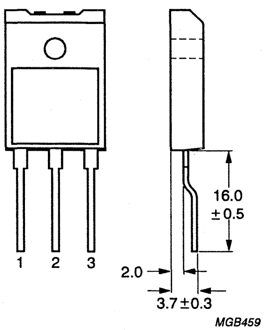
SOT199

Fig.13 Leadform 199-04.



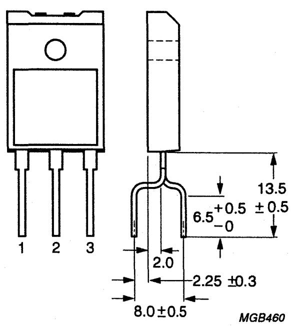
SOT199

Fig.14 Leadform 199-05.



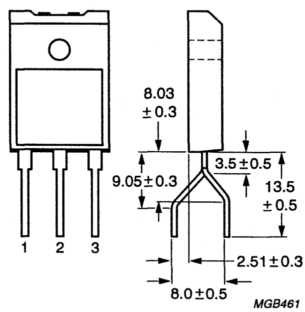
SOT199

Fig.15 Leadform 199-06.



SOT199

Fig.16 Leadform 199-08.



SOT199

Fig.17 Leadform 199-09.

MOUNTING INSTRUCTIONS

GENERAL DATA AND INSTRUCTIONS

General rules

1. Fasten the device to the heatsink before soldering the leads.
2. Avoid stress to the leads.
3. Keep mounting tool (e.g. screwdriver) clear of the plastic body.

Mounting methods

CLIP MOUNTING (TO126 AND SOT82)

Mounting with a spring clip gives:

a) A good thermal contact under the crystal area, and slightly lower thermal resistance than screw mounting.

b) Safe insulation for mains operation.

Minimum force for good heat transfer is 10 N.

Maximum force to avoid damaging the device is 80 N.

M2.5 AND M3 SCREW MOUNTING (TO126 ONLY)

It is recommended that a metal washer is inserted between the screw head and the device.

Do not use self-tapping screws.

Mounting torque for screw mounting:

Minimum torque for good heat transfer is 0.40 Nm.

Maximum torque to avoid damaging the device is 0.60 Nm.

When the driven nut is in direct contact with a toothed lock washer the torques are as follows:

Minimum torque for good heat transfer is 0.55 Nm.

Maximum torque to avoid damaging the device is 0.80 Nm.

BODY MOUNTING (SOT82)

The SOT82 envelope can be adhesive mounted or soldered onto a hybrid circuit.
For soldering, a copper plate or an anodised aluminium plate with a copper layer is recommended.

The device may be adhesive mounted directly onto a ceramic substrate.

Heatsink requirements

Minimum thickness: 2 mm.

Flatness in the mounting area: 0.02 mm maximum per 10 mm.

Mounting holes must be deburred, for further information see clip and screw mounting instructions.

Heatsink compound

The thermal resistance from mounting base to heatsink ($R_{th\ mb\text{-}h}$) can be reduced by applying a metallic oxide compound between the contact surfaces. Values given are of thermal resistance using this type of compound. Dow Corning 340 Heat sink compound is recommended. For insulated mounting, the compound should be applied to the bottom of both device and insulator.

Thermal data for heatsink mounting methods

Typical figures, for exact figures see data for each device type.

$R_{th\ mb\text{-}h}$	**Thermal resistance from mounting base to heatsink**	**K/W**	
Mounting method		**clip**	**screw**
TO126, direct with heatsink compound		1.0	0.5
TO126, direct without heatsink compound		3.0	1.0
TO126 with heatsink compound and 0.1 mm maximum mica insulator		3.0	3.0
TO126 without heatsink compound and 0.1 mm maximum mica insulator		6.0	6.0
SOT82, direct with heatsink compound		0.4	-
SOT82, direct without heatsink compound		2.0	-
SOT82 with heatsink compound and 0.1 mm maximum mica insulator		2.0	-
SOT82 without heatsink compound and 0.1 mm maximum mica insulator		5.0	-

Soldering

Recommendations for devices with a maximum storage temperature rating $T_{stg} \leq 150$ °C:

DIP OR WAVE SOLDERING.

Maximum permissible solder temperature is 260 °C at a distance from the body of > 5 mm and for a total contact time with soldering bath or waves of < 7 s.

HAND SOLDERING.

Maximum permissible temperature is 275 °C at a distance from the body of > 3 mm and for a total contact time with the soldering iron of < 5 s.

The body of the device must not touch anything with a temperature > 200 °C.

Avoid any force on body and leads during or after soldering; do not correct the position of the device or of its leads after soldering.

MOUNTING BASE SOLDERING.

Recommended metal-alloy of solder paste (85% metal weight)
62 Sn/36 Pb/2 Ag or 60 Sn/ 40 Pb.
Maximum soldering temperature 200˚C (tab temperature)
Maximum soldering cycle duration including preheating 30 s.

For good soldering and to avoid damage to the encapsulation, pre-heating at ≤ 165˚C for ≤ 10 s max is recommended.

Lead bending

Lead forming by Philips is available as an option on all products supplied in these outlines.

Maximum permissible tensile force on the body for 5 seconds is 20 N.

The leads can be bent, twisted or straightened. To keep forces within the above mentioned limits the leads should always be clamped rigidly near the body during bending. This is also to prevent damage to the seal of the leads within the plastic body.

Leads can be bent as near to the body as required, but adequate length should always be allowed for clamping. This is a minimum of 1.75 mm from the body to the start of a bend radius.

The internal radius of bend should never be less than the thickness of the lead. A minimum radius of at least 1.5 x lead thickness is preferred. See figure 1. Surface cracks in the dip tin coating on the lead are common when a radius less than 1.5 x lead thickness is used. Although exposing the copper material, these cracks do not affect the mechanical strength of the lead.

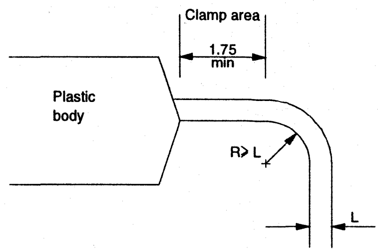
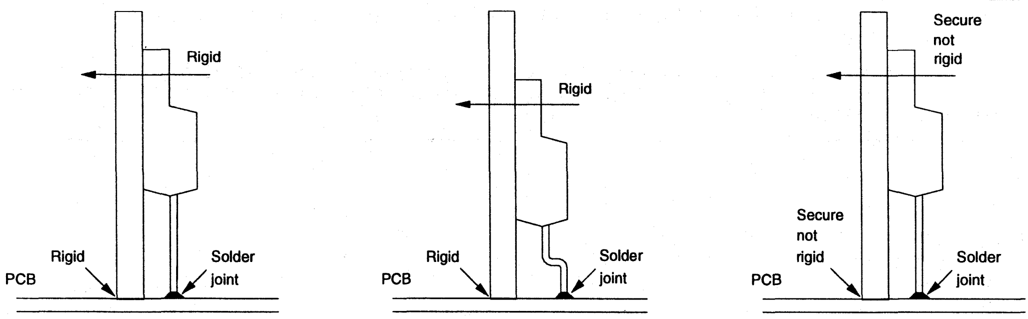


Fig 1. Minimum lead bend radius.

Additional guidelines

It is recommended that where a device is rigidly secured to a heatsink which is in turn rigidly secured to a PCB, that a bend is put in the leads to act as an expansion loop. This will prevent differential expansion of the mounting parts transferring stress to the soldering joint, as shown in figure 2 below. This is only necessary where the device is mounted so rigidly that expansion forces are transmitted through the assembly.



(a) Incorrect (b) Correct (c) Correct

Fig 2. Printed circuit board and heatsink mounting.

INSTRUCTIONS FOR CLIP MOUNTING

Direct mounting with spring clip

1. Apply heatsink compound to the mounting base, then place the device on the heatsink.
2. Push the short end of the clip into the narrow slot in the heatsink with the clip at an angle of 10° to 30° to the vertical. See figures 3 and 4.
3. Push down the clip over the device until the long end of the clip snaps into the wide slot in the heatsink. The clip should bear on the plastic body, not on the tab. See figure 5.

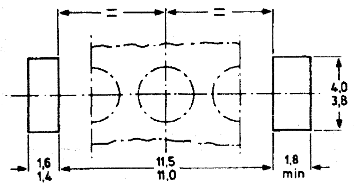


Fig 3. Heatsink requirements.

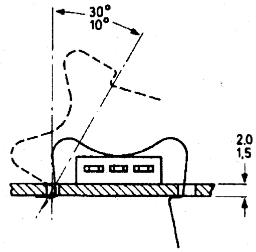


Fig 4. Mounting.

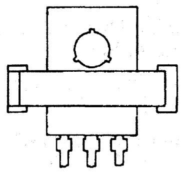


Fig 5. Position of device (top view).

Insulated mounting with clip and insulator

1. Apply heatsink compound to the bottom of both device and insulator, then place the device with the insulator on the heatsink.
2. Push the short end of the clip into the narrow slot in the heatsink with the clip at an angle of 10° to 30° to the vertical. See figures 6, 7 and 8.
3. Push down the clip over the device until the long end of the clip snaps into the wide slot in the heatsink. The clip should bear on the plastic body, not on the tab. Ensure that the device is centred on the mica insulator to prevent unwanted movement.

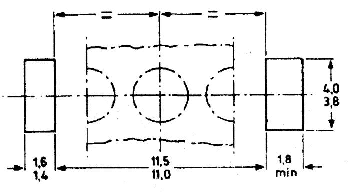


Fig 6. Heatsink requirements.

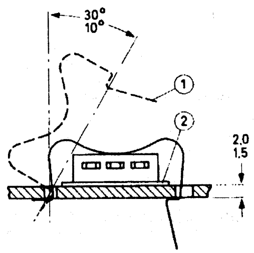


Fig 7. Mounting.
(1) spring clip
(2) insulator

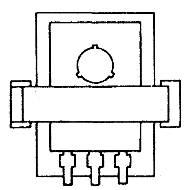


Fig 8. Position of device (top view).

INSTRUCTIONS FOR SCREW MOUNTING (TO126 ONLY)

Direct mounting with screw and spacing washer

THROUGH HEATSINK WITH NUT

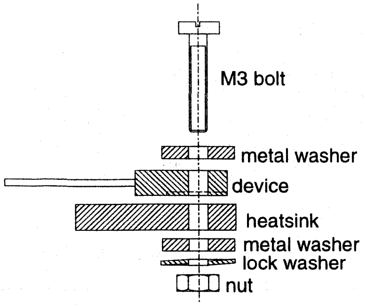


Fig 9. Assembly

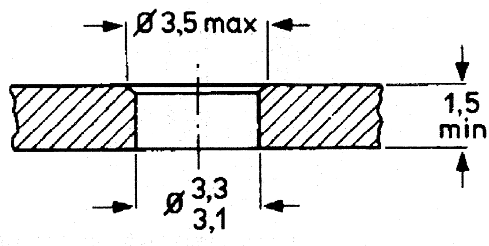


Fig 10. Heatsink requirements.

INTO TAPPED HEATSINK

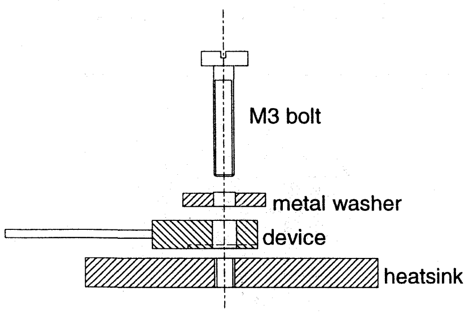


Fig 11. Assembly.

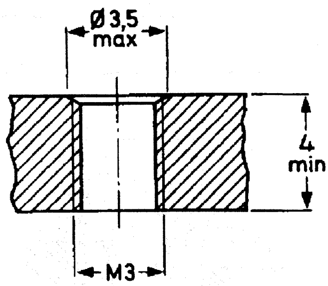


Fig 12. Heatsink requirements.

Insulated mounting with screw and spacing washer

Not recommended where mounting tab is at mains voltage.

THROUGH HEATSINK WITH NUT

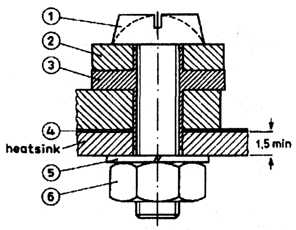


Fig 13. Insulated screw mounting with rectangular washer.

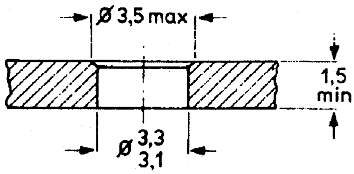


Fig 14. Heatsink requirements.

(1) M2.5 screw
(2) metal washer
(3) insulating bush
(4) insulating washer
(5) lock washer
(6) M2.5 nut

INTO TAPPED HEATSINK

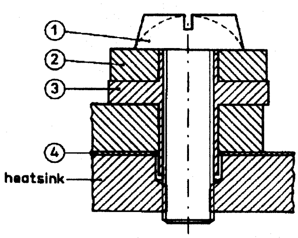


Fig 15. Insulated screw mounting with rectangular washer into tapped heatsink.

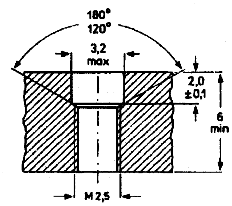


Fig 16. Heatsink requirements.

(1) M2.5 screw
(2) metal washer
(3) insulating bush
(4) insulating washer

GENERAL DATA AND INSTRUCTIONS

General rules

1. Fasten the device to the heatsink before soldering the leads.
2. Avoid stress to the leads.
3. Keep mounting tool (e.g. Screwdriver) clear of the plastic body.
4. When screw mounting, the rectangular washer should not exert any force on the plastic part of the body.

Mounting methods

CLIP MOUNTING

Mounting with a spring clip gives:

a) A good thermal contact under the crystal area, and slightly lower thermal resistance than screw mounting.

b) Safe insulation for mains operation.

Minimum force for good heat transfer is 10 N.

Maximum force to avoid damaging the device is 80 N.

M3 SCREW MOUNTING

It is recommended that a metal washer is inserted between screw head and mounting tab.

Do not use self-tapping screws.

Mounting torque for screw mounting:

For thread-forming screws these are final values.

Minimum torque for good heat transfer is 0.55 Nm.

Maximum torque to avoid damaging the device is 0.80 Nm.

When a nut or screw is driven directly against the tab, the torques are as follows:

Minimum torque for good heat transfer is 0.40 Nm.

Maximum torque to avoid damaging the device is 0.60 Nm.

RIVET MOUNTING NON-INSULATED.

The device should not be pop-rivetted to the heatsink. It is permissible to press-rivet the metal tab providing that eyelet rivets of soft material are used, and the press forces are slowly and carefully controlled.

This method is not permitted for full-pack envelopes (SOT186 and SOT186A) because it will damage the plastic encapsulation.

Heatsink requirements

Flatness in the mounting area: 0.02 mm maximum per 10 mm.
Mounting holes must be deburred, for further information see clip and screw mounting instructions.

Heatsink compound

The thermal resistance from mounting base to heatsink ($R_{th\ mb\text{-}h}$) can be reduced by applying a metallic oxide compound between the contact surfaces. Values given are of thermal resistance using this type of compound. Dow Corning 340 Heat sink compound is recommended. For insulated mounting, the compound should be applied to the bottom of both device and insulator.

Thermal data for TO220 envelopes with various heatsink mounting methods

Typical figures, for exact figures see data for each device type.

$R_{th\ mb\text{-}h}$ Thermal resistance from mounting base to heatsink	K/W	
Mounting method	**clip**	**screw**
direct with heatsink compound	0.3	0.5
direct without heatsink compound	1.4	1.4
with heatsink compound and 0.1 mm maximum mica insulator	2.2	-
with heatsink compound and 0.25 mm maximum alumina insulator	0.8	-
with heatsink compound and 0.05 mm mica insulator		
insulated up to 500 V	-	1.4
insulated up to 800 V / 1000 V	-	1.6
without heatsink compound and 0.05 mm mica insulator		
insulated up to 500 V	-	3.0
insulated up to 800 V / 1000 V	-	4.5

Additional insulators are generally not required when mounting the full-pack (SOT186 and SOT186A) envelopes.

Soldering

Recommendations for devices with a maximum storage temperature rating ≤ 175 ˚C:

DIP OR WAVE SOLDERING.

Maximum permissible solder temperature is 260 ˚C at a distance from the body of > 5 mm and for a total contact time with soldering bath or waves of < 7 s.

HAND SOLDERING.

Maximum permissible temperature is 275 °C at a distance from the body of > 3 mm and for a total contact time with the soldering iron of < 5 s.

The body of the device must not touch anything with a temperature > 200 °C.

It is not permitted to solder the metal tab of the device to a heatsink, otherwise the junction temperature rating will be exceeded.

Avoid any force on body and leads during or after soldering; do not correct the position of the device or of its leads after soldering.

Lead bending

Maximum permissible tensile force on the body for 5 seconds is 20 N.

The leads can be bent, twisted or straightened. To keep forces within the above mentioned limits the leads should always be clamped rigidly near the body during bending. This is also to prevent damage to the seal of the leads within the plastic body.

Leads can be bent as near to the body as required, but adequate length should always be allowed for clamping. This is a minimum of 1.75 mm from the body to the start of a bend radius.

The internal radius of bend should never be less than the thickness of the lead. A minimum radius of at least 1.5 x lead thickness is preferred. See figure 1. Surface cracks in the dip tin coating on the lead are common when a radius less than 1.5 x lead thickness is used. Although exposing the copper material, these cracks do not affect the mechanical strength of the lead. Lead forming by Philips is available as an option on all products supplied in these outlines.

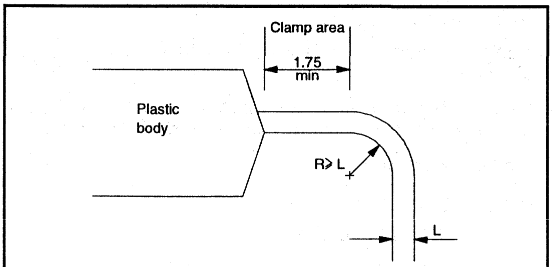


Fig 1. Minimum lead bend radius.

Additional guidelines

It is recommended that where a device is rigidly secured to a heatsink which is in turn rigidly secured to a PCB, that a bend is put in the leads to act as an expansion loop. This will prevent differential expansion of the mounting parts transferring stress to the soldering joint, as shown in figure 2 below. This is only necessary where the device is mounted so rigidly that expansion forces are transmitted through the assembly.

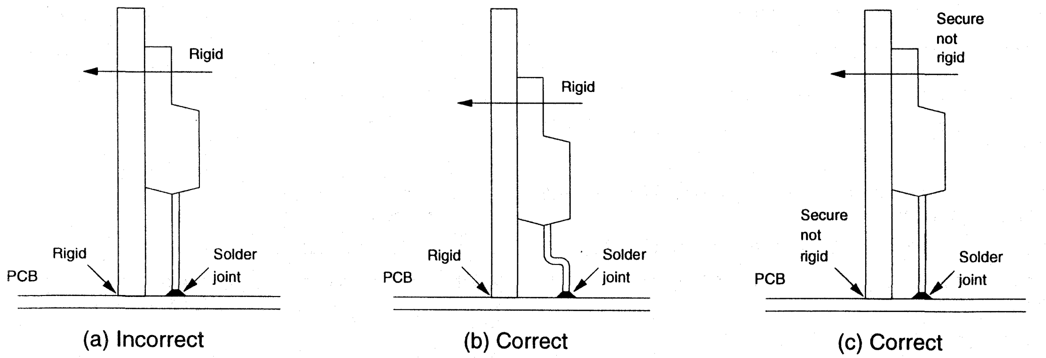


Fig 2. Printed circuit board and heatsink mounting.

INSTRUCTIONS FOR CLIP MOUNTING

Direct mounting with spring clip

1. Apply heatsink compound to the mounting base, then place the device on the heatsink.
2. Push the short end of the clip into the narrow slot in the heatsink with the clip at an angle of 10° to 30° to the vertical. See figures 3 and 4.
3. Push down the clip over the device until the long end of the clip snaps into the wide slot in the heatsink. The clip should bear on the plastic body, not on the tab. See figure 5.

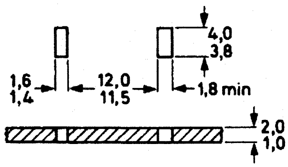


Fig 3. Heatsink requirements.

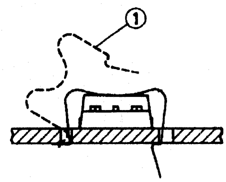


Fig 4. Mounting.
(1) spring clip.

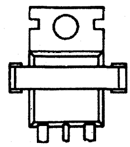


Fig 5. Position of device (top view).

Insulated mounting with spring clip

1. Apply heatsink compound to the bottom of both device and insulator, then place the device with the insulator on the heatsink.
2. Push the short end of the clip into the narrow slot in the heatsink with the clip at an angle of 10° to 30° to the vertical. See figures 6, 7 and 8.
3. Push down the clip over the device until the long end of the clip snaps into the wide slot in the heatsink. The clip should bear on the plastic body, not on the tab. Ensure that the device is centred on the mica insulator to prevent unwanted movement.

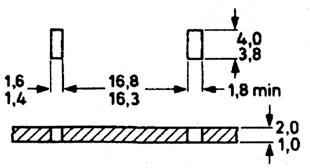


Fig 6. Heatsink requirements.

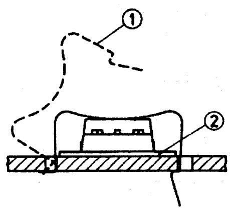


Fig 7. Mounting.
(1) spring clip.
(2) insulator.

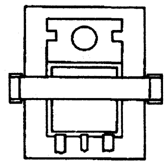


Fig 8. Position of device (top view).

INSTRUCTIONS FOR SCREW MOUNTING

Direct mounting with screw and spacing washer

THROUGH HEATSINK WITH NUT

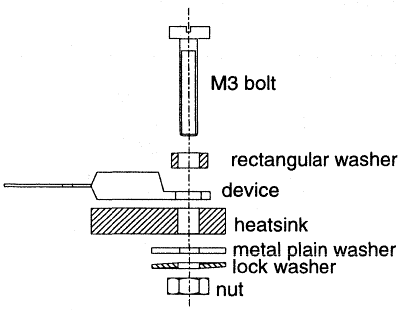


Fig 9. Assembly

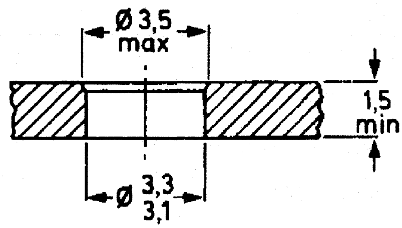


Fig 10. Heatsink requirements

INTO TAPPED HEATSINK

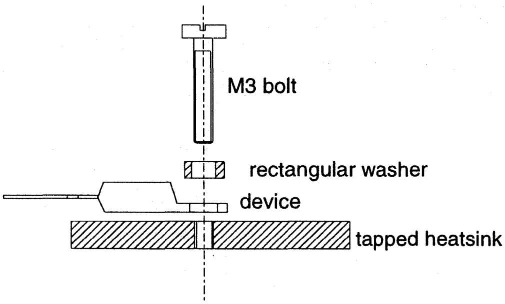


Fig 11. Assembly

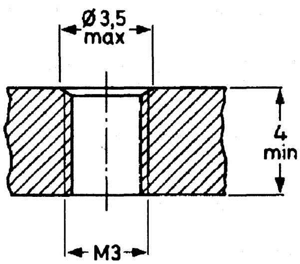


Fig 12. Heatsink requirements.

Insulated mounting with screw and spacing washer

Not recommended where mounting tab is at mains voltage. Not applicable for SOT186 or SOT186A.

THROUGH HEATSINK WITH NUT

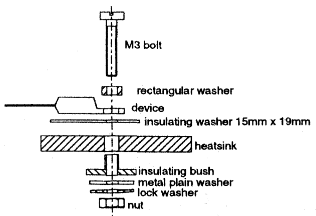


Fig 13. Insulated screw mounting with rectangular washer

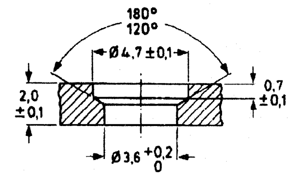


Fig 14. Heatsink requirements for 500 V insulation

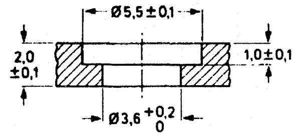


Fig 15. Heatsink requirements for 800V insulation

INTO TAPPED HEATSINK

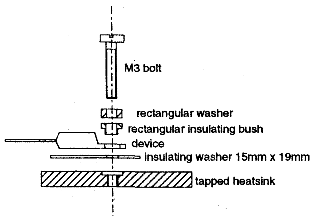


Fig 16. Insulated screw mounting with rectangular washer into tapped heatsink.

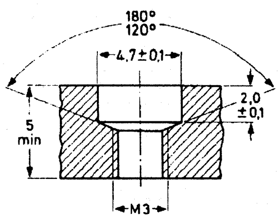


Fig 17. Heatsink requirements for 500 V insulation

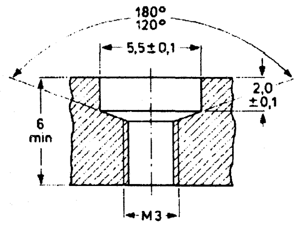
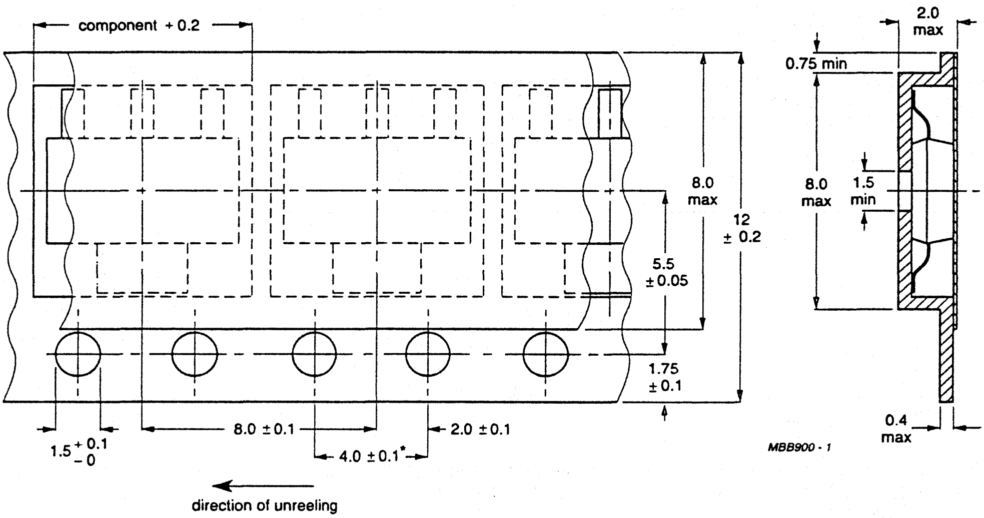


Fig 18. Heatsink requirements for 1000V insulation

TAPE and REEL PACKING (SOT223)

Tape and reel packing meets the feed requirements of automatic pick and place equipment (packing conforms to IEC publication 286). The tape is an ideal shipping container, making handling easy and providing secure blister cavities in which the transistors are sealed with peel-off cover tape.

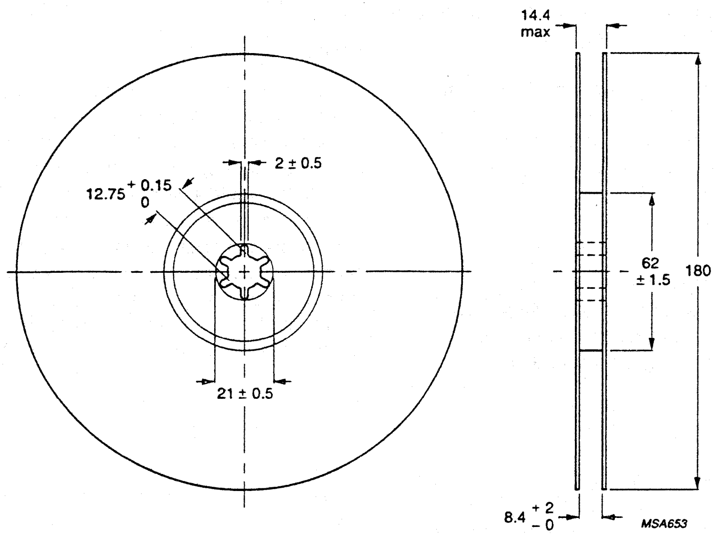
Packing quantities for SOT223 are 1000 pieces per 7-inch (180 mm) reel.



Dimensions in mm.

Tolerance over any 10 pitches: ±0.2 mm.

Fig.1 Specification for 12 mm tape, 7-inch reel (SOT223).



Dimensions in mm.

Fig.2 Reel for blister tape.

MOUNTING AND SOLDERING (SOT223)

Mounting methods

There are two basic forms of electronic component construction, those with leads for through-hole mounting and microminiature types for surface mounting (SMD). Through-hole mounting gives a very rugged construction and uses well established soldering methods. Surface mounting has the advantages of high packing density plus high-speed automated assembly. Surface mounting techniques are complex and this chapter gives only a simplified overview of the subject.

Not all electronic components are available as surface mounting types and this often leads to the mixing of through-hole with surface mounting components on one substrate (a mixed print). The mix of components affects the soldering methods that can be applied. A substrate having SMDs mounted on one or both sides but no through-hole components is likely to be suitable for reflow or wave soldering. A double-sided mixed print that has through-hole components and some SMDs on one side and densely packed SMDs on the other normally undergoes a sequential combination of reflow and wave soldering. When the mixed print has only through-hole components on one side and all SMDs on the other, wave soldering is usually applied.

Reflow soldering

This is the preferred soldering technique for SOT223 components.

SOLDER PASTE

Most reflow soldering techniques utilize a paste that is a mixture of flux and solder. The solder paste is applied to the substrate before the components are placed. It is of sufficient viscosity to hold the components in place and, therefore, an application of adhesive is not required. Drying of the solder paste by preheating increases the viscosity and prevents any tendency for the components to become displaced during the soldering process. Preheating also minimizes thermal shock and drives off flux solvents.

Screen printing

This is the best high-volume production method of solder paste application. An emulsion-coated, fine mesh screen with apertures etched in the emulsion to coincide with the surfaces to be soldered is placed over the substrate. A squeegee is passed across the screen to force solder paste through the apertures and on to the substrate. The layer thickness of screened solder paste is usually between 150 and 200 μm.

Stencilling

In this method a stencil with etched holes to pass the paste is used. The thickness of the stencil determines the amount of amount of solder paste that is deposited on the substrate. This method is also suited to high-volume work.

Dispensing

A computer-controlled pressure syringe dispenses small doses of paste to where it is required. This method is mainly suitable for small production runs and laboratory use.

Pin transfer

A pin picks up a droplet of solder paste from a reservoir and transfers it to the surface of the substrate or component. A multi-pin arrangement with pins positioned to match the substrate is possible and this speeds up the process time.

REFLOW TECHNIQUES

Thermal conduction

The prepared substrates are carried on a conveyor belt, first through a preheating stage and then through a soldering stage. Heat is transferred to the substrate by conduction through the belt. Figure 3 shows a theoretical time/temperature relationship for thermal conduction reflow soldering. This method is particularly suited to thick film substrates and is often combined with infrared heating.

Infrared

An infrared oven has several heating elements giving a broad spectrum of infrared radiation, normally above and below a closed loop belt system. There are separate zones for preheating, soldering and cooling. Dwell time in the soldering zone is kept as short as possible to prevent damage to components and substrate. A typical heating profile is shown in Fig.4. This reflow method is often applied in double-sided prints.

Vapour phase

A substrate is immersed in the vapours of a suitable boiling liquid. The vapours transfer latent heat of condensation to the substrate and solder reflow takes place. Temperature is controlled precisely by the boiling point of the liquid at a given pressure. Some systems employ two vapour zones, one above the other. An elevator tray, suspended from a hoist mechanism passes the substrate vertically through the first vapour zone into the secondary soldering zone and then hoists it out of the vapour to be cooled. A theoretical time/temperature relationship for this method is shown in Fig.5.

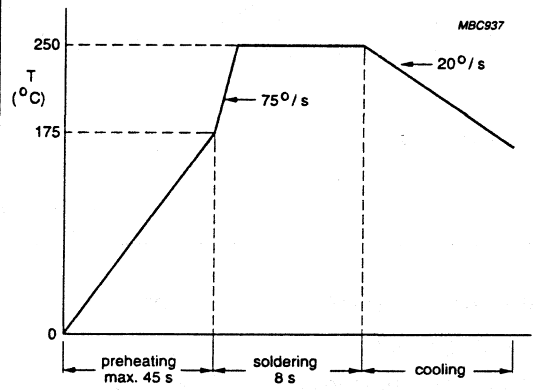


Fig.3 Theoretical time/temperature curve for a typical thermal conduction reflow cycle.

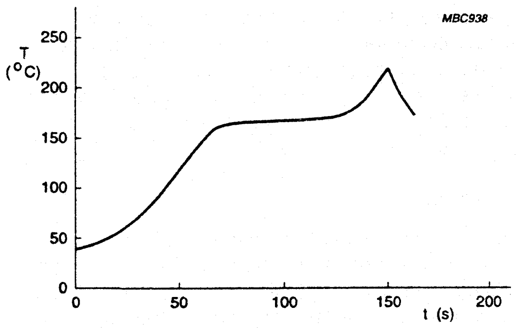


Fig.4 Typical temperature profile of an infrared oven operating at a belt speed of 0.41 m/min.

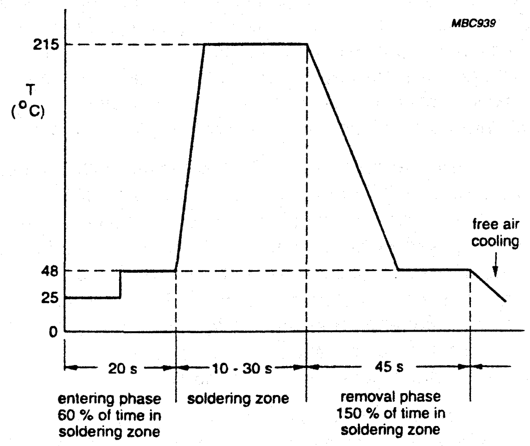


Fig.5 Theoretical time/temperature curve relationship for dual vapour reflow soldering.

Wave soldering

This soldering technique can be applied to SOT223 components.

ADHESIVE APPLICATION

Since there are no connecting wires to retain them, leadless and short-leaded components are held in place with adhesive for wave soldering. A spot of adhesive is carefully placed between each SMD and the substrate. The adhesive is then heat-cured to withstand the forces of the soldering process, during which the components are fully immersed in solder. There are several methods of adhesive application.

Pin transfer method

A pin is used to transfer a droplet of adhesive from a reservoir to a precise position on the surface where it is required. The size of the droplet depends on pin diameter, depth to which the pin is dipped in the reservoir, rheology of the adhesive, and the temperature of adhesive and surrounds. The pin can be part of a pin array (bed of nails) that corresponds exactly with the required adhesive positions on the substrate. With this method, adhesive can be applied to the whole of one side of a substrate in one operation and is therefore suitable for high-volume production and can be used with pre-loaded mixed prints.

Alternatively, pins can be used to transfer adhesive to the components before they are placed on the substrate. This adds flexibility to production runs where variations in layout must be accommodated.

Screen printing method

A fine mesh screen is coated with emulsion except in the positions where the adhesive is required to pass. The screen is placed on the substrate and a squeegee passing across it forces adhesive through the uncoated parts of the screen. The amount of adhesive printed-through depends on the size of the uncoated screen areas, the thickness of the screen coating, the rheology of the adhesive and various machine parameters. With this method, the substrate must be flat and pre-loaded mixed prints cannot be accommodated.

Pressure syringe method

A computer-controlled syringe dispenses adhesive from an enclosed reservoir by means of pulses of compressed air. The adhesive dot size depends on the size of the syringe nozzle, the duration and pressure of the pulsed air and the viscosity of the adhesive. This method is most suited to low volume production. An advantage is the flexibility provided by computer programmability.

Fluxing

The quality of the soldered connections between components and substrate is critical for circuit performance and reliability. Flux promotes solderability of the connecting surfaces and is chosen for the following attributes:

- Removal of surface oxides
- Prevention of reoxidation
- Transference of heat from source to joint area
- Residue that is non-corrosive or, if residue is corrosive, should be easy to clean away after soldering
- Ability to improve wettability (readiness of a metal surface to form an alloy at its interface with the solder) to ensure strong joints with low electrical resistance
- Suitability for the desired method of flux application.

In wave soldering, liquified flux is usually applied as a foam, a spray or in a wave.

Foam

Flux foam is made by forcing low-pressure, water-free clean air through an aerator immersed in liquid flux. Fine bubbles of flux are directed onto the substrate/component surfaces where they burst and form a thin, even layer. The flux also penetrates any plated-through holes. The flux has to be chosen for its foaming capabilities.

Spray

Several methods of spray fluxing exist, the most common involves a mesh drum rotating in liquid flux. Air is blown into the drum which, when passing through the fine mesh, directs a spray of flux onto the underside of the substrate. The amount of flux deposited is controllable by the speed of the substrate passing through the spray, the speed of rotation of the drum and the density of the flux.

Wave

A wave fluxer creates a double flowing wave of liquid flux which adheres to the surface as the substrate passes through. Wave height control is essential and a soft wipe-off brush is usually incorporated to remove excess flux from the substrate.

Pre-heating

Pre-heating of the substrate and components is performed immediately before soldering. This reduces thermal shock as the substrate enters the soldering process, causes the flux to become more viscous and accelerates the chemical action of the flux and so speeds up the soldering action.

Soldering

Wave soldering is usually the best method to use when high throughput rates are required. The single-wave soldering principle (Fig.6) is the most straight forward method and can be used on simple substrates with two-terminal SMD components. More complex substrates with increased circuit density and closer spacing of conductors can pose the problems of nonwetting (dry joints) and solder bridging. Bridging can occur across the closely spaced leads of multi-leaded devices as well as across adjacent leads on neighbouring components. Nonwetting is usually caused by components with plastic bodies. The plastic is not wetted by solder and creates a depression in the solder wave, which is augmented by surface tension. This can cause a shadow behind the component and prevent solder from reaching the joint surfaces. A smooth laminar solder wave is required to avoid bridging and a high pressure wave is needed to completely cover the areas that are difficult to wet. These conflicting demands are difficult to attain in a single wave but dual wave techniques go a long way in overcoming the problem.

In a dual wave machine (Fig.7), the substrate first comes into contact with a turbulent wave which has a high vertical velocity. This ensures good solder contact with both edges of the components and prevents joints from being missed. The second smooth laminar wave completes the formation of the solder fillet, removes excess solder and prevents bridging. Figure 8 indicates the time/temperature relationship measured at the soldering site in dual wave soldering.

New methods of wave soldering are developing continually. For example, the Omega System is a single wave agitated by pulses, which combines the functions of smoothness and turbulence. In another, a lambda wave injects air bubbles in the final part of the wave. A further innovation is the hollow jet wave in which the solder wave flows in the opposite direction to the substrate.

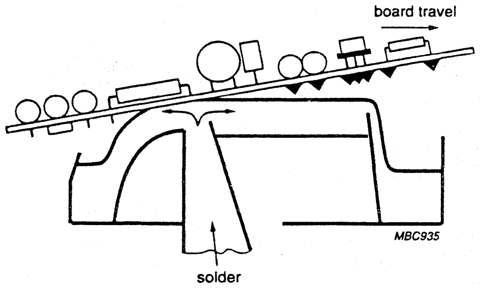


Fig.6 Single wave soldering principle.

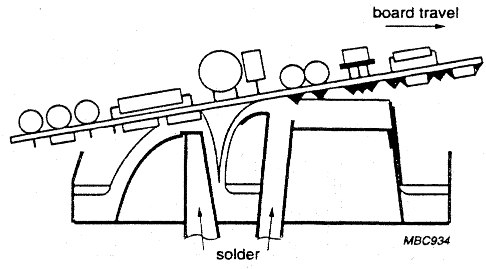


Fig.7 Dual wave soldering principle.

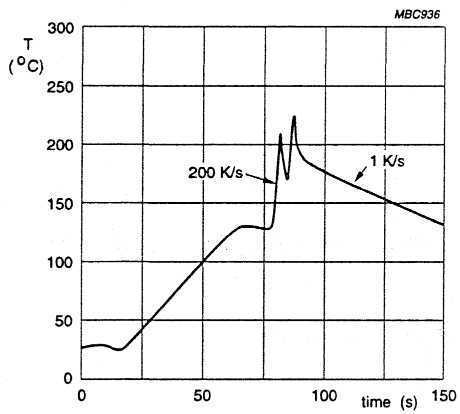


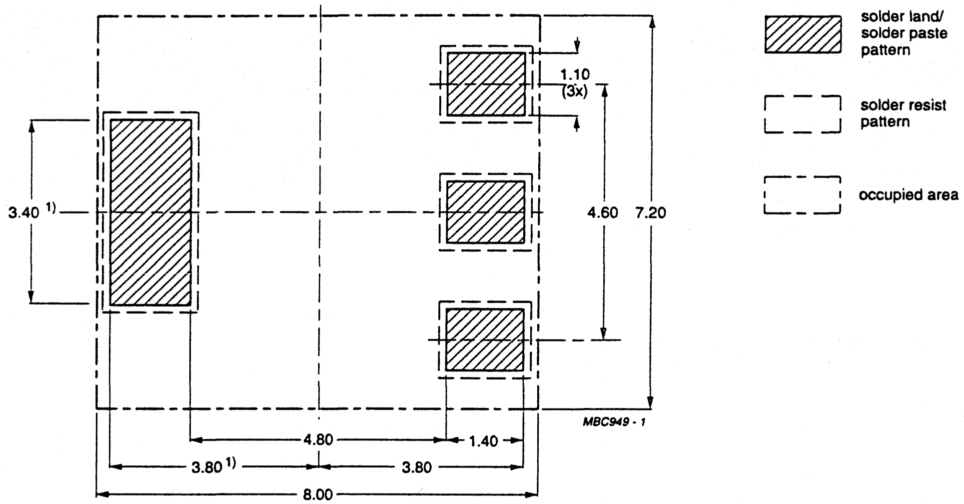
Fig.8 Typical time-temperature curve measured at the soldering site.

Footprint design

The footprint design of a component for surface mounting is influenced by many factors:

- Features of the component, its dimensions and tolerances
- Circuit board manufacturing processes
- Desired component density
- Minimum spacing between components
- Circuit tracks under the component
- Component orientation (if wave soldering)
- Positional accuracy of solder resist to solder lands
- Positional accuracy of solder paste to solder lands (if reflow soldering)
- Component placement accuracy
- Soldering process parameters
- Solder joint reliability parameters.

SOT223 FOOTPRINTS

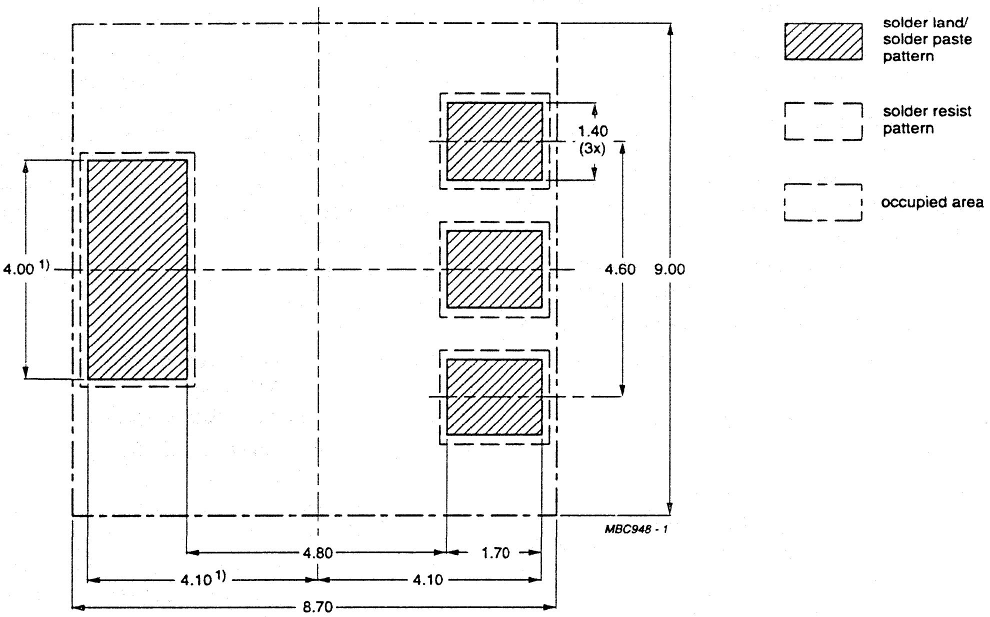


Dimensions in mm.

Placement accuracy: ±0.25 mm.

1) To improve the power dissipation the marked dimensions may be enlarged without changing the solder resist cut out of the footprint.

Fig.9 Reflow soldering footprint for SOT223; typical dimensions.



Dimensions in mm.

Placement accuracy: ±0.25 mm.

1) To improve power dissipation the marked dimensions may be enlarged without changing the solder resist cut out of the footprint.

Fig.10 Wave soldering footprint for SOT223; typical dimensions.

Hand soldering microminiature components

It is possible to solder microminiature components with a light-weight hand-held soldering iron, but this method has obvious drawbacks and should be restricted to laboratory use and/or incidental repairs on production circuits:

- Hand-soldering is time-consuming and therefore expensive
- The component cannot be positioned accurately and the connecting tags may come into contact with the substrate and damage it
- There is a risk of breaking the substrate and internal connections in the component could be damaged
- The component envelope could be damaged by the soldering iron.

THERMAL CONSIDERATIONS

Thermal resistance

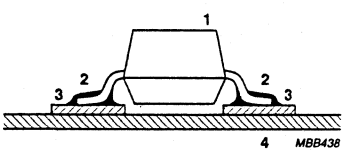
Circuit performance and long-term reliability are affected by the temperature of the transistor die. Normally, both are improved by keeping the die temperature (junction temperature) low.

Electrical power dissipated in any semiconductor device is a source of heat. This increases the temperature of the die about some reference point, normally an ambient temperature of 25 °C in still air. The size of the increase in temperature depends on the amount of power dissipated in the circuit and the net thermal resistance between the heat source and the reference point.

Devices lose most of their heat by conduction when mounted on a substrate. Referring to Fig.11, heat conducts from its source (the junction) via the envelope leads and soldered connections to the substrate. Some heat radiates from the envelope into the surrounding air where it is dispersed by convection or by forced cooling air. Heat that radiates from the substrate is dispersed in the same way.

The elements of thermal resistance shown in Fig.12 are defined as follows:

$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base
$R_{th\ j\text{-}c}$	thermal resistance from junction to case
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point
$R_{th\ s\text{-}a}$	thermal resistance from soldering point to ambient
$R_{th\ c\text{-}a}$	thermal resistance from case to ambient ($R_{th\ s\text{-}a}$ and $R_{th\ c\text{-}a}$ are the same for most envelopes)
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient.



Heat radiates from the envelope (1) to ambient.

Heat conducts via leads (2), solder joints (3) to the substrate (4).

Fig.11 Heat losses.

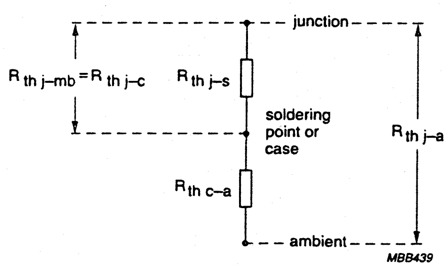


Fig.12 Representation of thermal resistance paths of a device mounted on a substrate or printed board.

The temperature at the junction depends on the ability of the envelope and its mounting to transfer heat from the junction region to the ambient environment. The basic relationship between junction temperature and power dissipation is:

$$T_{j\ max} = T_{amb} + P_{tot\ max}(R_{th\ j\text{-}s} + R_{th\ s\text{-}a})$$
$$= T_{amb} + P_{tot\ max}(R_{th\ j\text{-}a})$$

where

$T_{j\ max}$ is the maximum junction temperature

T_{amb} is the ambient temperature

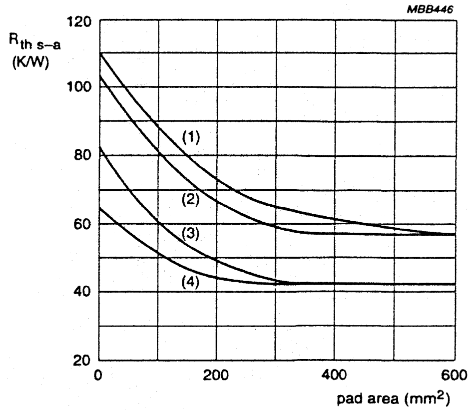
$P_{tot\ max}$ is the maximum power handling capability of the device, including the effects of external loads when applicable.

In the expression for $T_{j\ max}$, only T_{amb} and $R_{th\ s\text{-}a}$ can be varied by the user. The package mounting technique and the flow of cooling air are factors that affect $R_{th\ s\text{-}a}$. The device power dissipation can be controlled to a limited extent but under recommended usage, the supply voltage and circuit loading dictate a fixed power maximum. The $R_{th\ j\text{-}s}$ value is essentially independent of external mounting method and cooling air; but is sensitive to the materials used in the envelope construction, the die bonding method and the die area, all of which are fixed.

Values of $T_{j\ max}$ and $R_{th\ j\text{-}s}$ or $R_{th\ j\text{-}c}$ are given in the device data sheets. For applications where the temperature of the case is stabilized by a large or temperature-controlled heatsink, the junction temperature can be calculated from $T_j = T_{case} + P_{tot} \times R_{th\ j\text{-}c}$ or, using the soldering point definition, from $T_j = T_{solder} + P_{tot} \times R_{th\ j\text{-}s}$.

Thermal resistance ($R_{th\ s\text{-}a}$ and $R_{th\ c\text{-}a}$)

The thermal resistance from soldering point to ambient and that from case to ambient depends on the shape and material of the tracks and substrate as illustrated in Figs 13 and 14. Standard mounting conditions to set the maximum power ratings of the SOT223 envelope are shown in Fig.15. This shows single-sided 35 µm copper-clad epoxy fibre-glass print, 1.5 mm thick. the tracks are fully solder-tinned and the shaded areas shown are copper.



(1) single-sided, unplated
(2) single-sided, plated
(3) double-sided, unplated
(4) double-sided, plated.

Fig.13 Thermal resistance ($R_{th\ s\text{-}a}$) as a function of pad area on different configurations of FR4 epoxy fibre-glass circuit board.

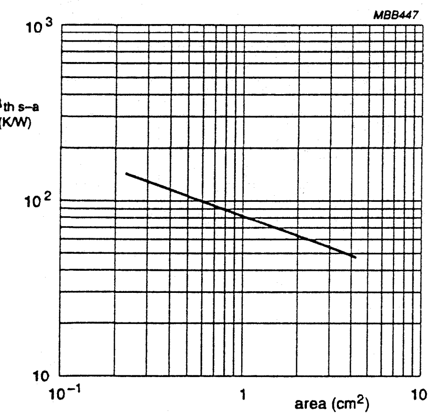


Fig.14 Thermal resistance ($R_{th\ s\text{-}a}$) as a function of area of ceramic substrate.

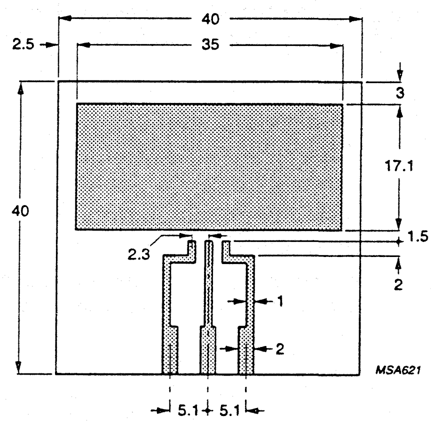


Fig.15 Test circuit for SOT223.

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Data handbook system

DATA HANDBOOK SYSTEM

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